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Service Manual

Memory 64K

P4500-25

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PHILIPS DATA SYSTEMS
SERV. DOC. AND TRAINING DEPT.
P.O. Box 245, APELDOORN,
THE NETHERLANDS.

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1 GENERAL DESCRIPTION

1. GENERAL DESCRIPTION

The Main Memory of the P4500 is a 32K word dynamic MOS Random Access Memory which features user-transparent error correction. The memory is based on the MOSTEK MK4116-4 16K bit RAM chip, which requires refreshing within 2ms, used in an array of 21 chips for the 16K 16-bit word PCB (including 5 bits used for internal error checking and correcting) or 42 chips for the full 32K16 version. The 32K word version will be normally implemented. Up to 8 modules may be connected to the System Bus, providing a total memory capacity of 512K bytes (8 x 32K x 16 bits). A strap on the card distinguishes whether the card is used in UPL or P851 mode. It must be in the P851 mode if it is installed in a P4500 system and a P851 control Unit is present also.

The organization of the memory in 16 bit "words" has no effect on the byte organization of the P4500 system. It is possible to read or write a 'word' or either left or right 'character', the timing and control for these various possibilities being provided by the memory itself.

Power failure detection and battery back-up facilities are optionally available at system level to save the memory contents in case of power failure. On the WMA-1 logic diagrams, all devices marked with a 'B' are sypplied with battery back-up voltage. Read/Write memory cycles are forbidden during this time.

The refresh action is performed, as far as possible, "hidden" to avoid possible timing clashes with the master units on the System Bus but it is ensured that all memory cells are refreshed within 2ms. Refresh is performed completely independent of the P4500 system.

The memory modules are implemented on multi-layer PCB's which interface with the System Bus via a standard 32 pin connector requiring no further connections or cabling.

The WMA-1 memory features normal access times in the region of 630ns, cycle times around 700ns (except Write Character) to the memory interface (about 1300ns at Bus level) and is fully TTL compatible.

TYPES OF TRANSFERS

There are six possible types of transfer indicated by a combination of WRITE, CHA and MAD15 signals as illustrated in the table below:

WRITE	CHA	MAD15	OPERATION
1	0	Don't care	The 16 bit word on BIO(00-15)N is written at the given address.
1	1	0	The right-hand character on BIO(8-15)N is written into the left character position of the given address.
1	1	1	The right-hand character on BIO(8-15)N is written into the right character position of the given address.
0	0	Don't care	The 16 bit word is read out onto BIO(00-15)N
0	1	0	The left-hand character is read out onto the right character position on BIO(8-15)N.
0	1	1	The right-hand character is read out onto the right character position on BIO(8-15)N.

Table 1.1 CYCLE MODE CONTROL SIGNALS

These various types of transfer are laid out in simplified form in Figure 1.1 Simplified Data Transfer. In this diagram, the letters refer to the multiplexors and latches described in detail in the Logic Description part. For the purpose of this diagram, blocks F and G refer to latches, B, D, E, and J are multiplexors, A, C and H are buffers and ECC is the Error Correction Chip.

Note that a memory cycle always reads or writes a complete 16 bit word so, for example, to write a right-character, it is required to read the word, correct the data out if necessary, substitute the right character with the new data from BIO(8-15)N and write the new word, and error correction bits, back into the same memory location.

Note also that all character transfer to and from memory is via BIO(8-15)N.

Figure 1.2 gives a layout of the WMA-1 PCB.

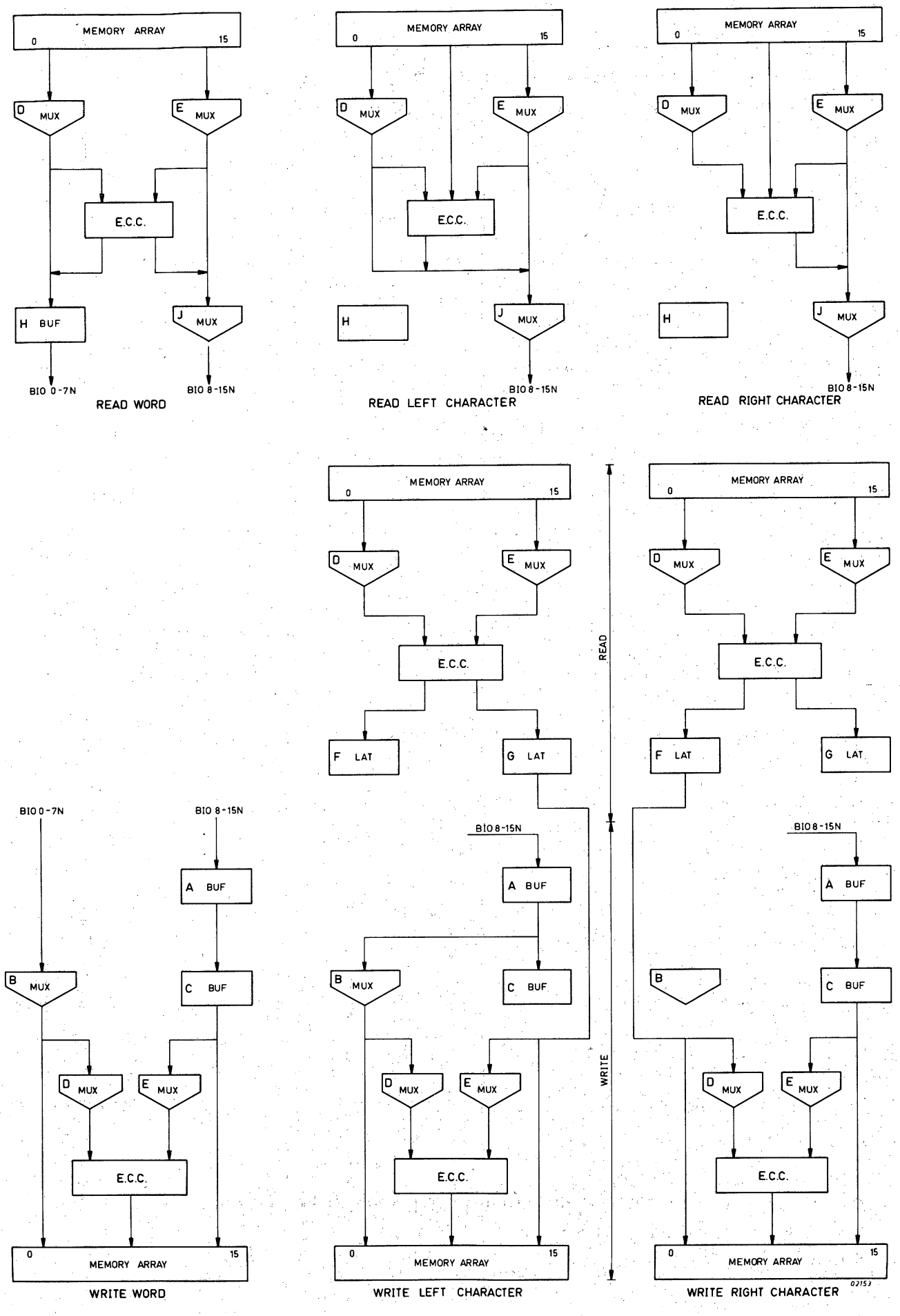


Figure 1.1 SIMPLIFIED DATA TRANSFER

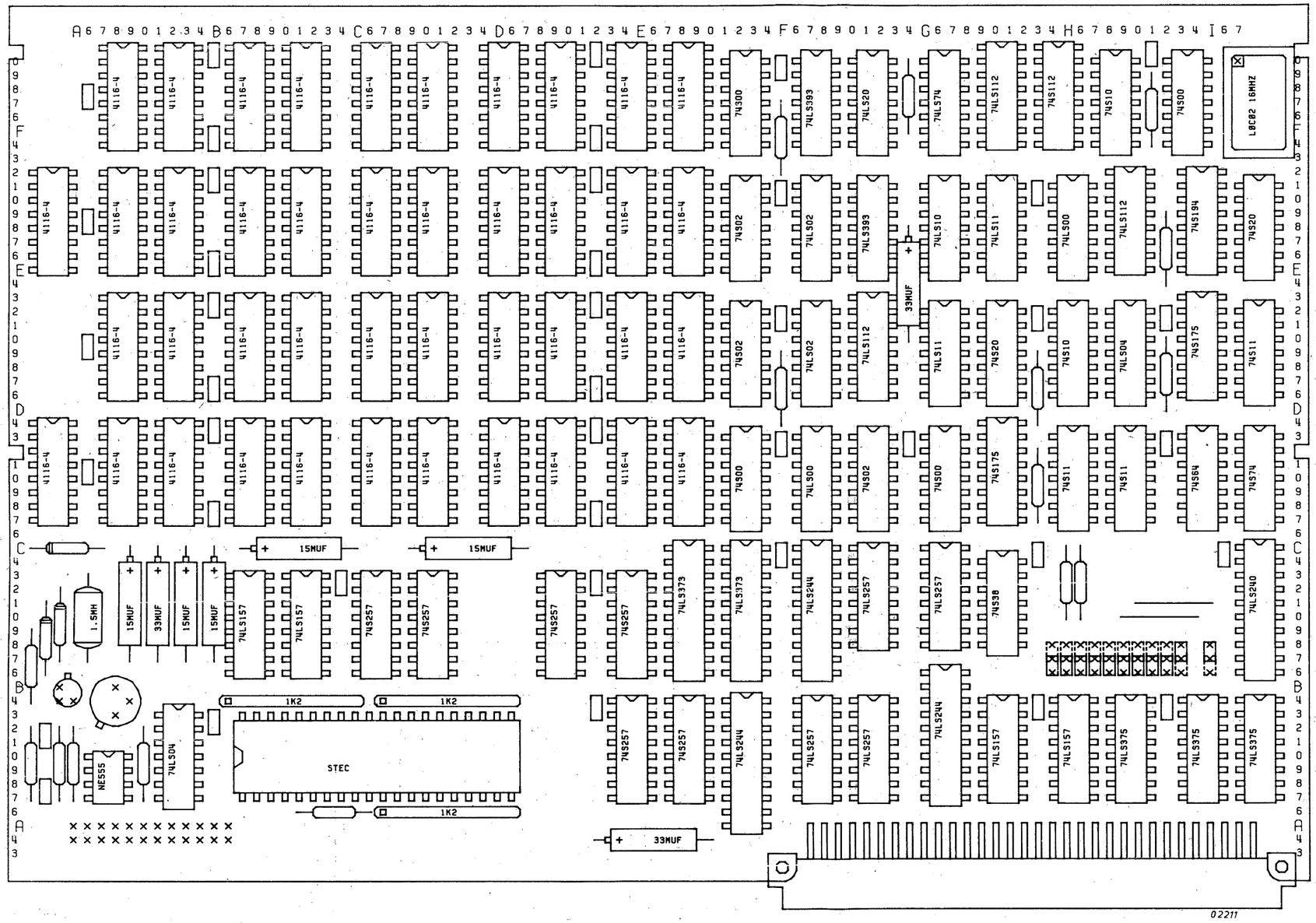


Figure 1.2 LAYOUT OF WMA-1 PCB

2 INTERFACE

2. INTERFACE

Tables 2.1 and 2.2 give the list of interface signals between the memory WMA-1 and the System Bus, their layout on the connector and a short description of each. Note that signals ending in 'N' are active (ie., perform their function) when in the 'LOW' state, (ie., is set to the logical "0" state) if they are control signals and represent the complement of their true value if they are data or address signals.

Note also that control signals (those which cause an immediate action upon their change of state) are always either a logical "0" or a logical "1", whereas data signals are also permitted to adapt indeterminate levels (high impedance state) when the information is not actually being used in the cycle.

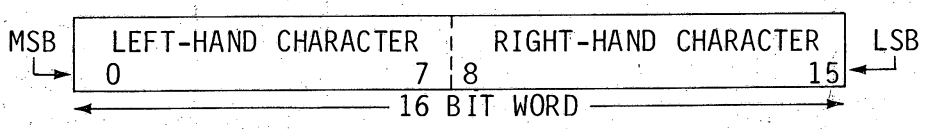
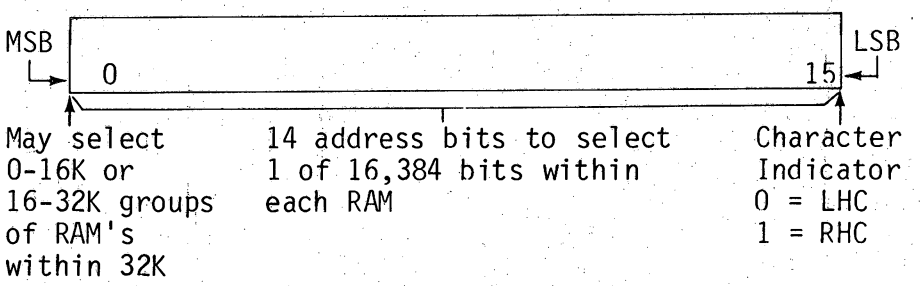
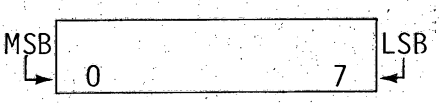
PGP BUS SIGNAL	DESCRIPTION
BIO(00-15)N	16 data lines used to transfer data between the memory and other system elements dealing with the interchange of data. 
MAD(00-15)	16 address lines which, during a master-memory exchange, provide addressing signals for the RAM chips, indicate (in character mode) which character is active and may select an "upper" and "lower" 16K within a 32K memory "block". 
MADE(0-7)	8 address extension lines to select memory capacities greater than 32K up to a maximum of 512K words. 
TMRN	A control signal originating in the Master to validate the data on the BIO(00-15)N, WRITE, CHA, MAD(0-7) lines and control the exchange.
TSMN	A control signal originating in the memory to indicate to the master that, in the case of a write cycle, the data has been written into the memory or, if a read cycle, that valid data is now present on the BIO lines
RSLN	A signal to indicate that the power levels are not in tolerance.
CHA	A control signal transmitted to the memory from the master which has control of the bus to indicate the type of operation as follows: CHA = 0 defines word operation CHA = 1 defines character operation
WRITE	A control signal transmitted from master to memory to indicate the type of operation as follows: WRITE = 0 defines read from memory WRITE = 1 defines write into memory

Table 2.1 INTERFACE SIGNAL DESCRIPTION

PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME	PIN NUMBER	SIGNAL NAME
1C01		1B01		1A01	
1C02	+5VM	1B02		1A02	+5VM
1C03		1B03		1A03	
1C04		1B04	0V	1A04	
1C05		1B05		1A05	
1C06	0V	1B06	ØKØ	1A06	0V
1C07		1B07	ØKI	1A07	RSLN
1C08		1B08		1A08	
1C09	0V	1B09		1A09	0V
1C10		1B10		1A10	TSMN
1C11		1B11	0V	1A11	TMRN
1C12	0V	1B12	MADE0	1A12	0V
1C13	MAD00	1B13	MADE1	1A13	MAD01
1C14	MAD02	1B14	0V	1A14	MAD03
1C15	MAD04	1B15	MADE2	1A15	MAD05
1C16	MAD06	1B16	MADE3	1A16	MAD07
1C17	MAD08	1B17	MADE4	1A17	MAD09
1C18	MAD10	1B18	MADE5	1A18	MAD11
1C19	MAD12	1B19	MADE6	1A19	MAD13
1C20	MAD14	1B20	MADE7	1A20	MAD15
1C21	CHA	1B21	0V	1A21	WRITE
1C22	0V	1B22		1A22	0V
1C23	BI008N	1B23		1A23	BI000N
1C24	BI009N	1B24		1A24	BI001N
1C25	BI010N	1B25		1A25	BI002N
1C26	BI011N	1B26	0V	1A26	BI003N
1C27	BI012N	1B27		1A27	BI004N
1C28	BI013N	1B28		1A28	BI005N
1C29	BI014N	1B29		1A29	BI006N
1C30	BI015N	1B30		1A30	BI007N
1C31	+12VM	1B31	+5VL	1A31	+12VM
1C32	+5VL	1B32	+5VL	1A32	+5VL

Table 2.2 INTERFACE SIGNALS

3 STRAP SETTING

3. STRAP SETTING

There are a total of 13 straps on this PCB, all located around co-ordinates B7H9. Two of them are soldered wires while the rest are plastic caps, (see figure 3.1).

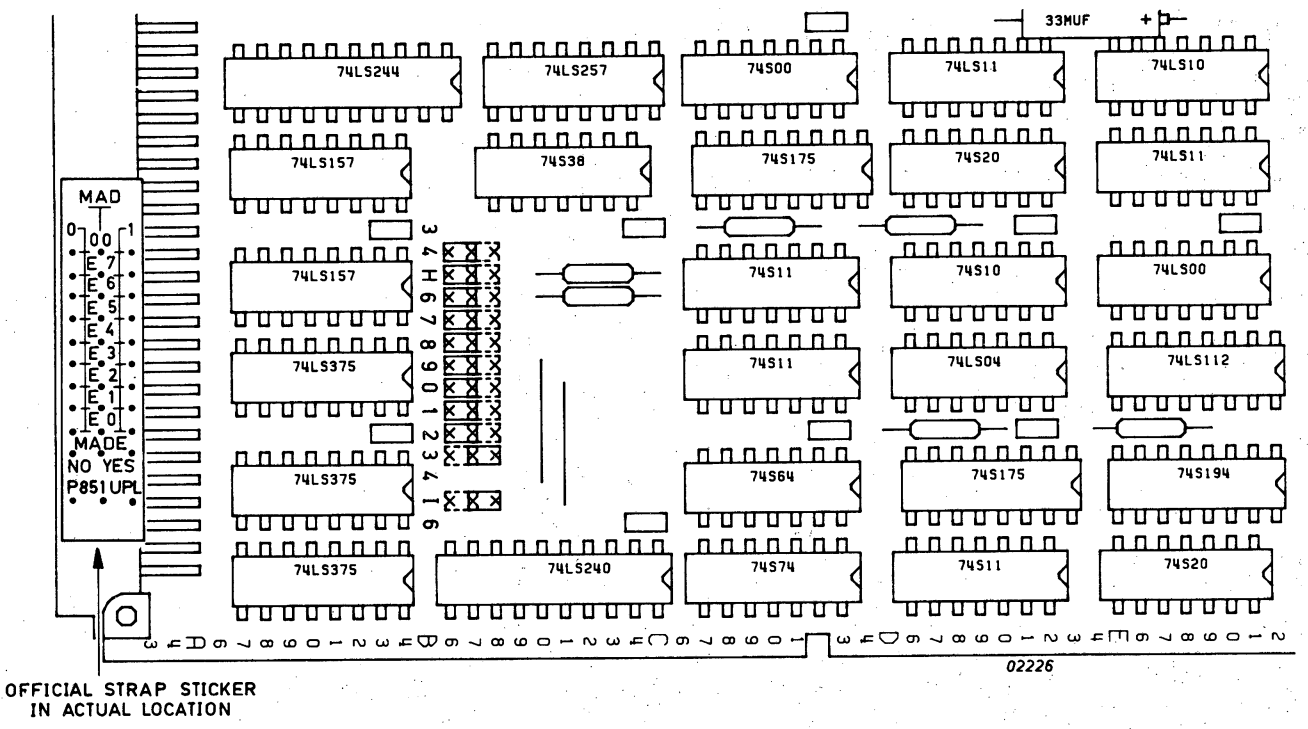


Figure 3.1 STRAP LOCATIONS

The soldered wire straps have the following meanings:

Strap on 'Y' co-ordinates C0 is for signal AOSEL

Strap on 'Y' co-ordinates C1 is for signal AD00

32K Module: Strap I4C0 to H9C0 (as shown)
and I0C1 to I5C1 (as shown)

16K Module: Strap I5C0 to I0C0
and H9C1 to I4C1

The plastic capped straps have the following meaning and signal names:

Co-ordinates		B6	B7	B8	MEANING		
		Pin 1	Pin 2	Pin 3	Pin1	Pin 2	Pin 3
	4	ADLOON	ADSOO	ADLOO	0	MADOO	1
	5	ADLE7N	ADSE7	ADLE7	0	MADE7	1
H	6	ADLE6N	ADSE6	ADLE6	0	MADE6	1
	7	ADLE5N	ADSE5	ADLE5	0	MADE5	1
	8	ADLE4N	ADSE4	ADLE4	0	MADE4	1
	9	ADLE3N	ADSE3	ADLE3	0	MADE3	1
	0	ADLE2N	ADSE2	ADLE2	0	MADE2	1
	1	ADLE1N	ADSE1	ADLE1	0	MADE1	1
I	2	ADLEON	ADSEO	ADLEO	0	MADEO	1
	3	H'	CASEL	EXT	=1	#CARDS	>1
	4						
	5	FSM	L	P851M	P851	MODE	UPL

NOTE: The numbers refer to the PCB's on figure 3.2 - examples of module addressing such that module (1) on figure 3.3 has the straps as shown in 1 below.

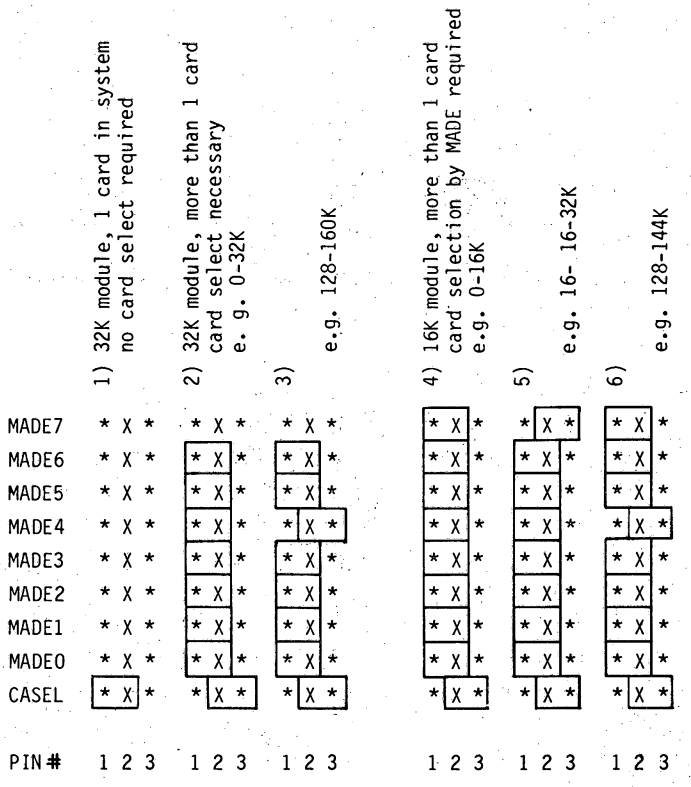
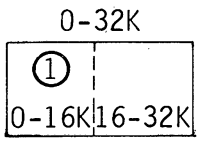


FIGURE 3.2 EXAMPLES OF THE USE OF THE STRAPS

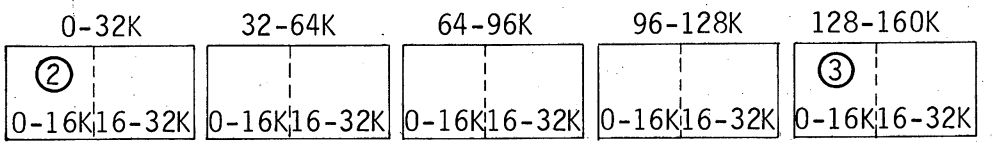
Note: Encircled numbers (e.g. ①) refer to strap layout on figure 3.3

a) 1 x 32K Module - No card selection necessary



MAD00 = Selection of upper or lower 16K on the PCB.

b) >1 x 32K Module - Card selection by MADE(0-7)



1) MAD00 = Upper/Lower 16K

2) MADE = Card Select

c) >2 x 16K Module - Card selection by combination of MAD00 and MADE

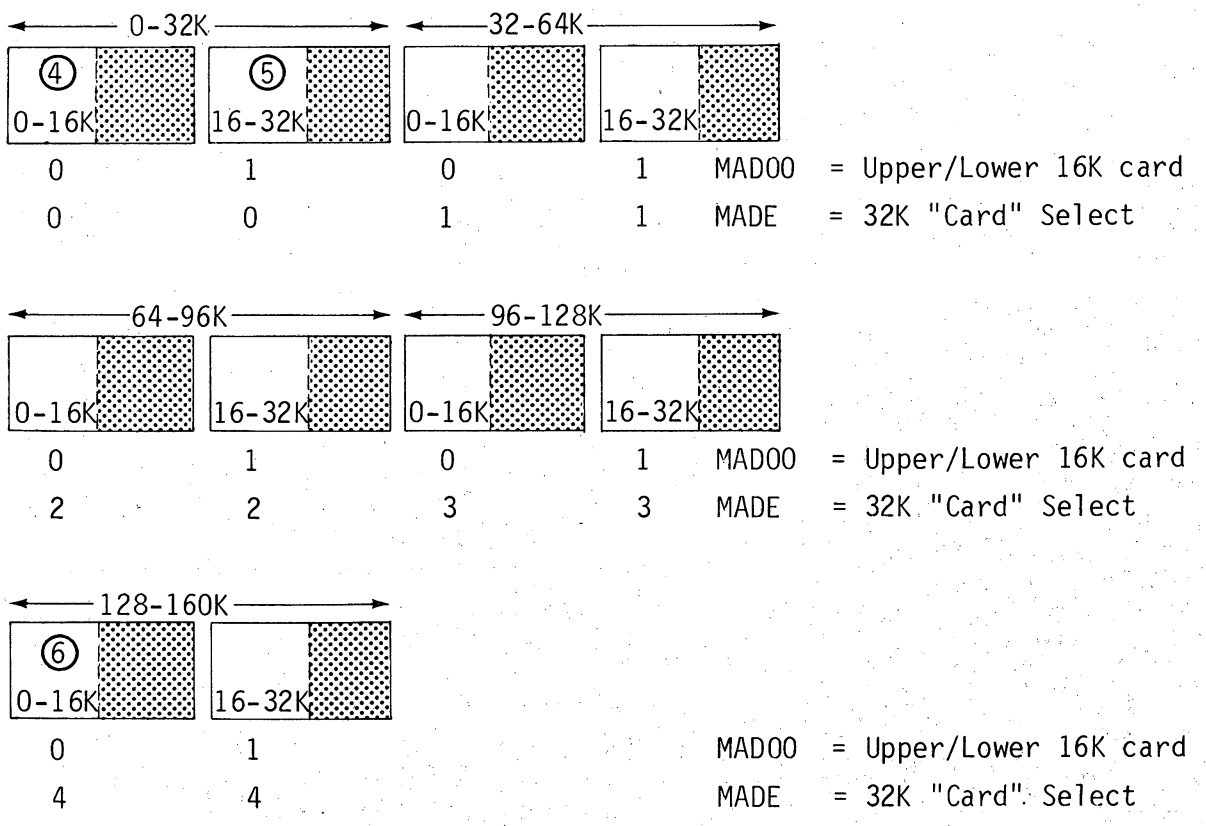


Figure 3.3 EXAMPLES OF MODULE ADDRESSING

4 HANDLING OF MOS MEMORY MODULES

4. HANDLING OF MOS MEMORY MODULES

Note that special care must be taken when handling, repairing or packaging MOS memory modules due to the build-up of static, which may occur and possibly discharge on one pin, thus damaging the device. It is therefore essential to prevent any difference in potential voltage between an MOS device and any surface, tool or person with which it may come into contact. The following rules may be helpful:

a) PACKAGING

MOS circuit boards may be packaged in a metal box, a wooden case, a cardboard box, or conductive plastic, but not in ordinary plastic. These conductive, or semi-conductive, materials prevent static discharge at one point.

b) REPAIRING

It is preferable that all work on MOS devices is carried out on a metal surface, which is in some way connected to ground. All tools and the device should remain on this surface throughout and the personnel must 'discharge' themselves on it before work commences. All electrical equipment used (e.g. 'scopes, digital voltmeters and the tip of the soldering iron) must be earthed.

c) PERSONNEL

It is advisable for personnel to 'ground' themselves before touching MOS devices, e.g. by touching a metal pipe that is earthed, or at least discharge themselves to the same potential as the working surface before commencing work.

5 RAM DESCRIPTION

5. RAM DESCRIPTION

The RAM used in the P4500 memory uses a device manufactured by Mostek (MK4116P-4). The features are:

a) 16,384 x 1 bit organisation
b) standard 16-pin package
c) standard +12V, +5V, -5V power supplies required
d) low power - 462mW active, 20mW standby
e) all inputs (including clocks) and output TTL compatible
f) 128 refresh cycles every 2 msecs
g) output data controlled by $\overline{CAS}$ and unlatched at the end of the cycle
h) access time 250 nsec, read/write cycle time 410 nsecs

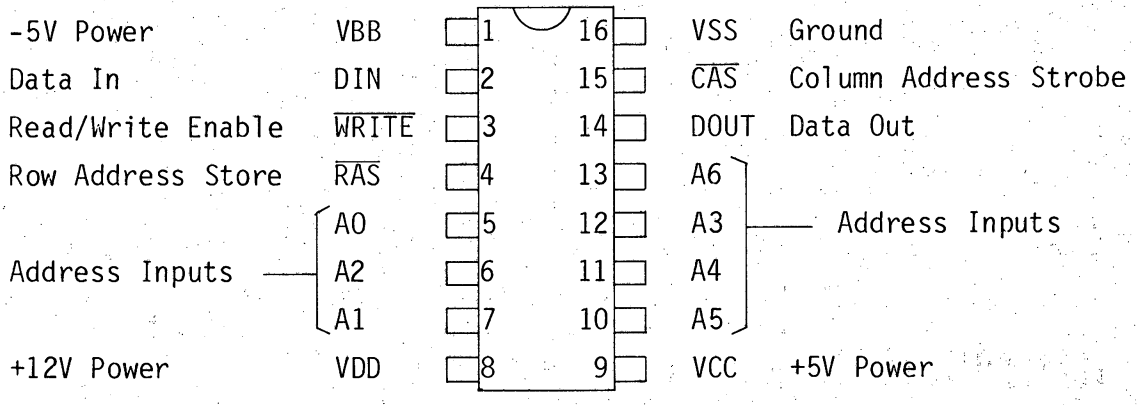


Figure 5.1 RAM PIN CONFIGURATION

The following pages indicate internal chip timing relationships for Read Cycle (figure 5.3), Write Cycle (figure 5.4) and Refresh Cycle (figure 5.5), as well as a simplified Block Diagram of the RAM (figure 5.2).

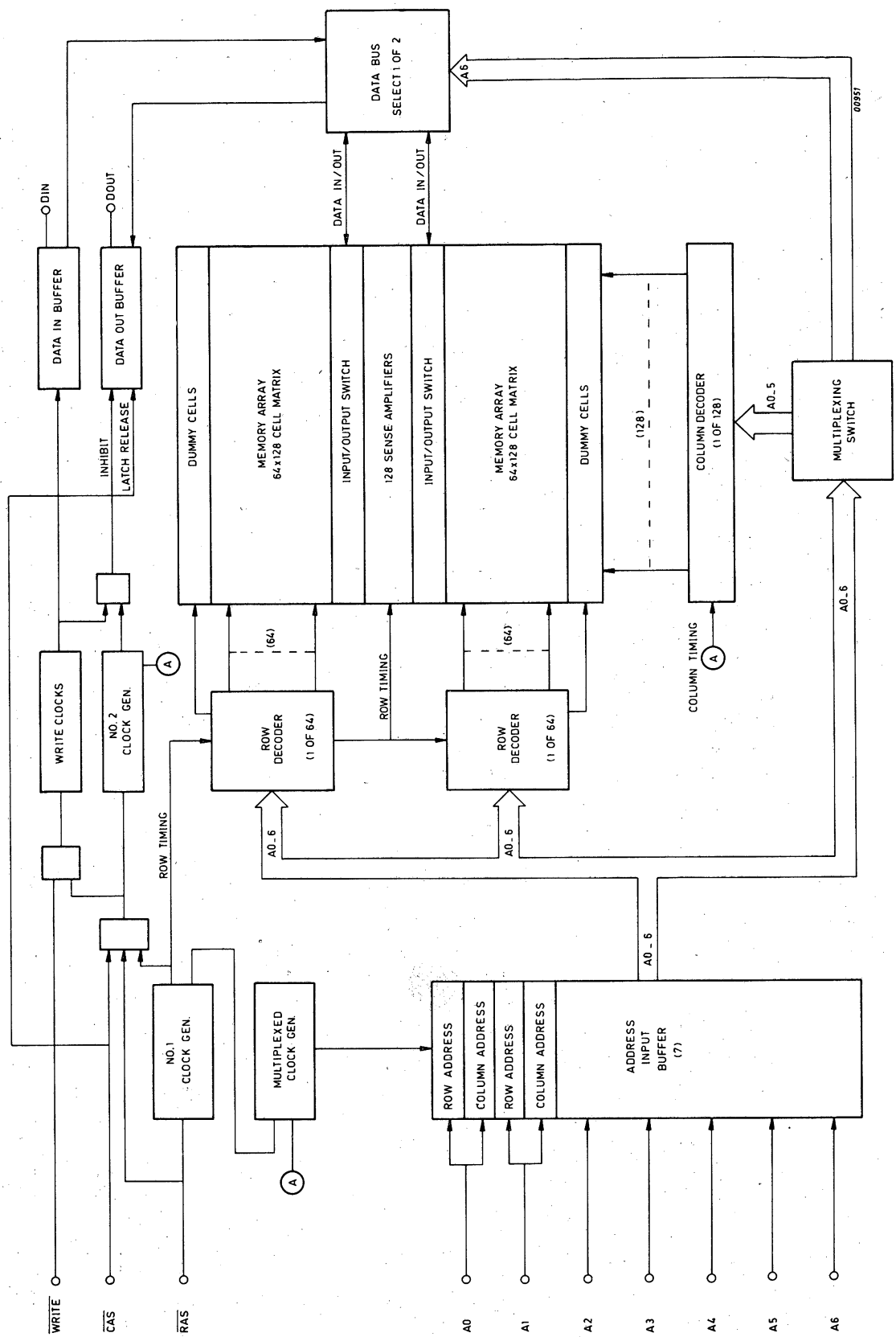


Figure 5.2 RAM BLOCK DIAGRAM

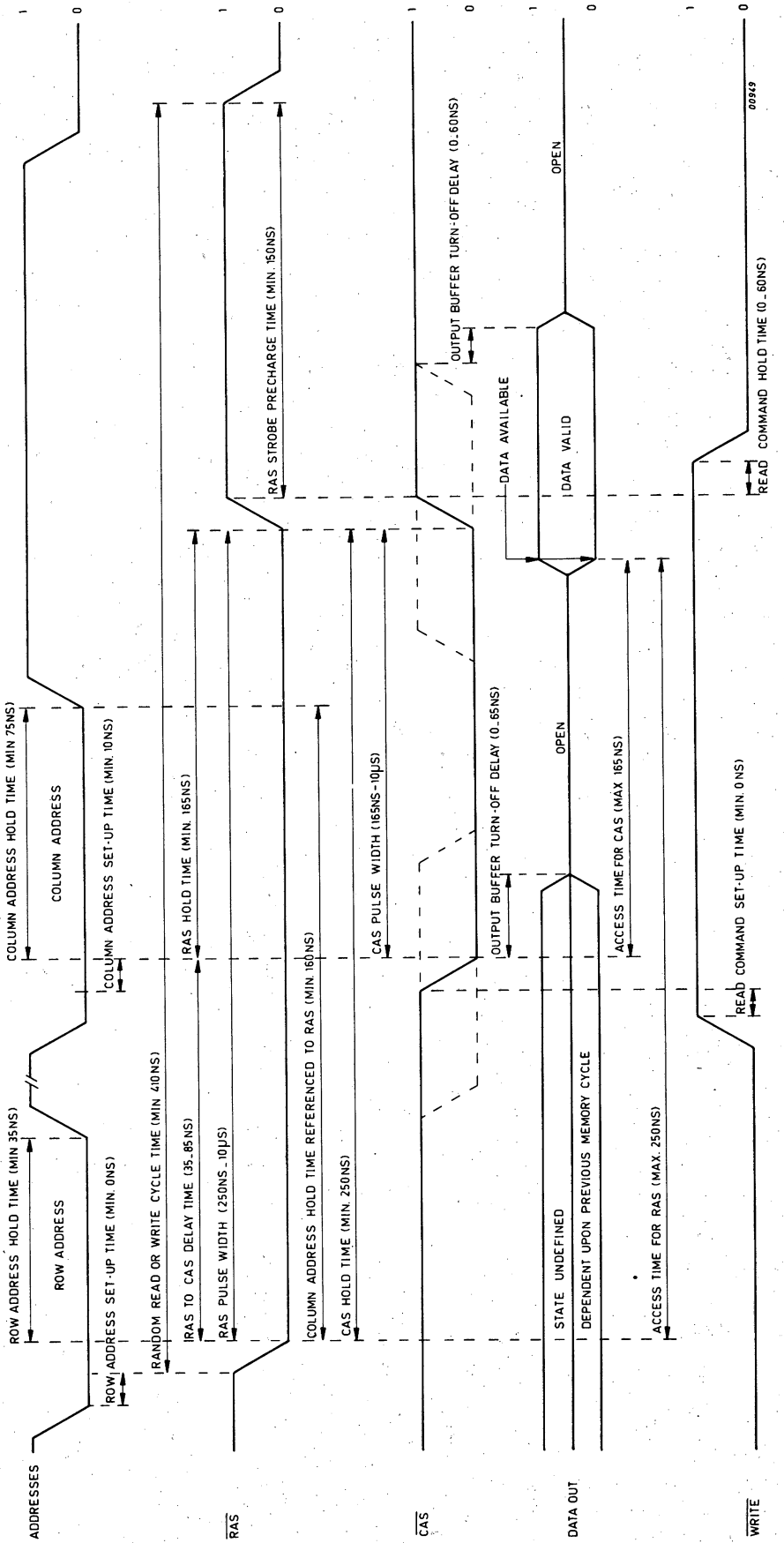


Figure 5.3 READ CYCLE TIMING DIAGRAM

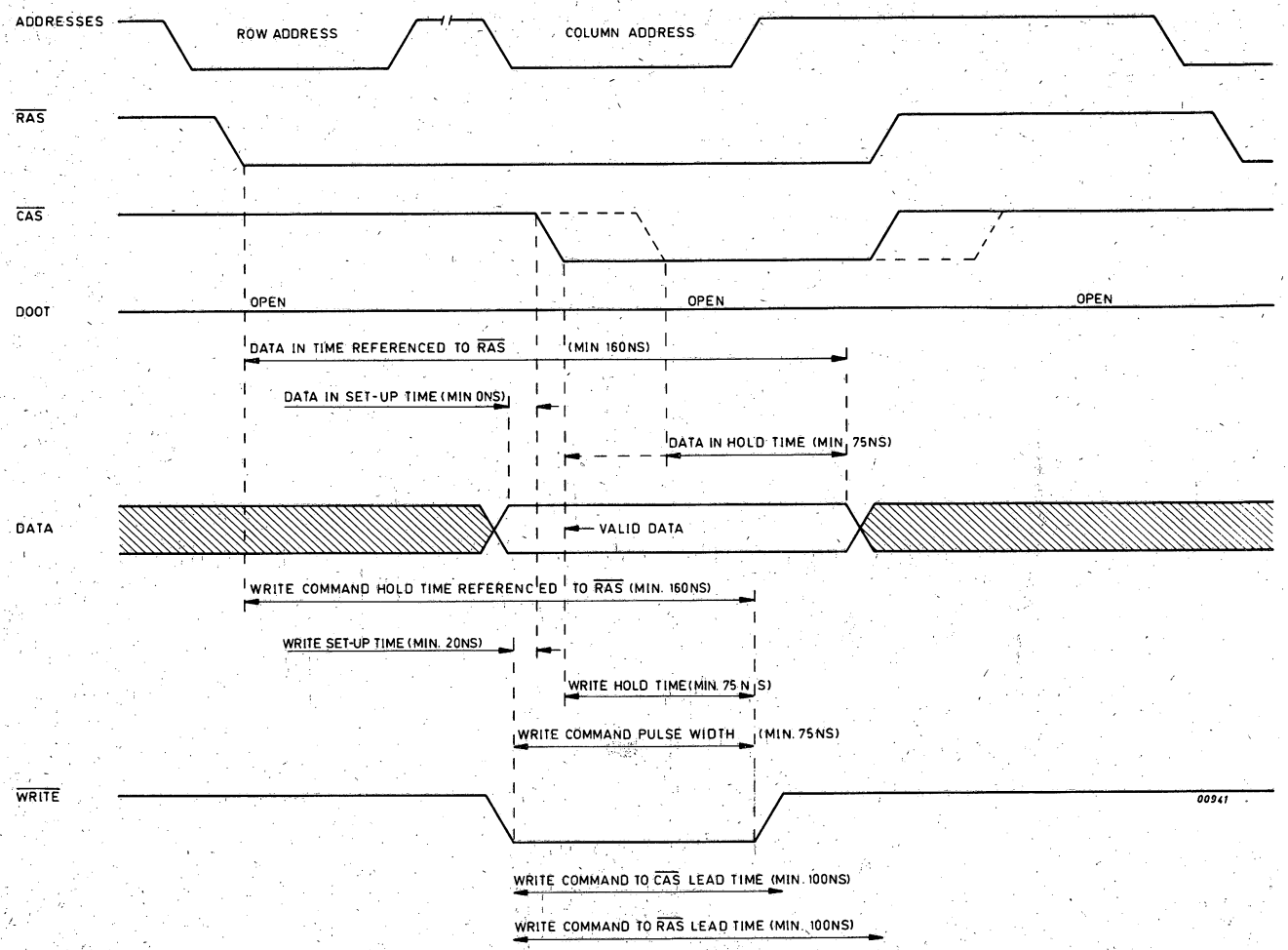


Figure 5.4 WRITE CYCLE TIMING DIAGRAM

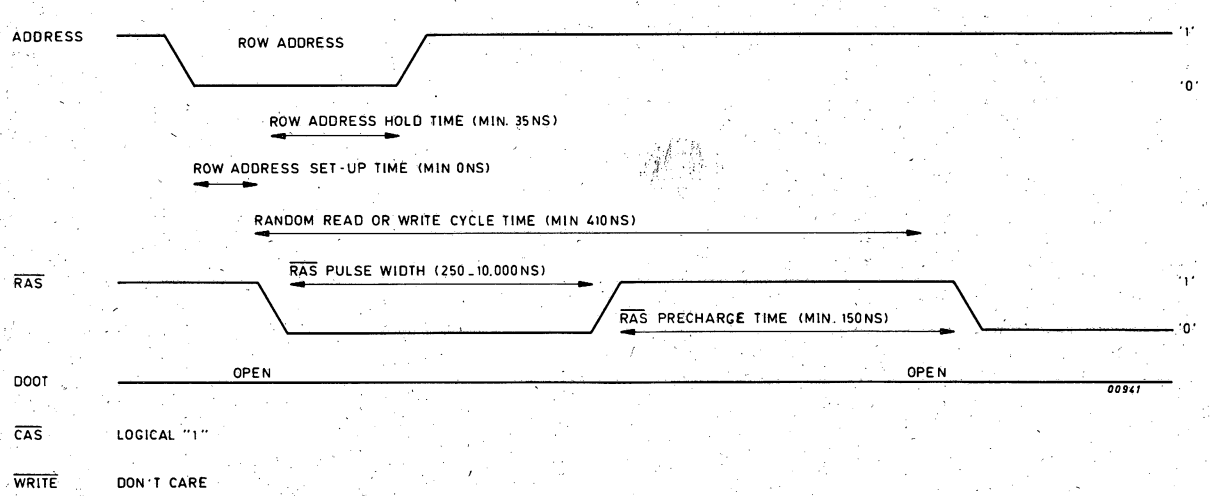


Figure 5.5 REFRESH CYCLE TIMING DIAGRAM

6 LOGIC DESCRIPTION

SECTION	6.1	GENERAL	PAGE 6-1
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	6.5	DATA IN/OUT	6-14
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	6.7	TIMING REFRESH CYCLE	6-29
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	6.9	P851 MODE	6-34

6.1 GENERAL

As mentioned previously, there are six different forms of memory cycle - Read/Write of Word/Left Character/Right Character. The following diagrams illustrate a simplified data flow for each of the six cycles described in the following text. Table 6.1 displays the various control signals necessary for each of these cycles.

a) WRITE WORD CYCLE - See figure 6.1

Data is made available on the BIO lines 00-15(N). The most significant (left-hand) character is enabled at multiplexor B by ELCHN being low and selected by CHAV being low. The least significant (right-hand) character is enabled through buffers A and C and then all 16 bits (MDIO-15) are selected by multiplexors D and E (by ENDATN and RWDS both being low), to the Error Connection Chip. At the same time as the data is presented to the memory array as MDI(0-15), the output of the ECC (the correction bits, MDIS 0-4) is also presented to the memory array and strobed into the required address by WEN (Write Enable). Latches F and G are disabled and buffer H and multiplexor J are put into the high impedance state.

b) READ WORD CYCLE - See figure 6.2

Data is read out of the memory array as MDØ 0-15 and the error correction bits MDØS 0-4. Multiplexors D and E gate MDØ 0-15 to the ECC (by RWDS being high) and also to the data out buffers H and J. When the ECC has checked the data and found it good, SFN remains high and the ECC takes over, driving the data onto BIO 00-15N via TRDØLN and TRDØRN both being low. If the ECC discovers a single bit error, it sets SFN low, corrects the data and drives the corrected data onto BIO 00-15N. Latches F and G are once again disabled.

c) READ LEFT CHARACTER - See figure 6.3

This cycle is very nearly identical to the Read Word Cycle except that the character mode enables latch G and disables the corresponding input buffer C. Note that although B - and in read word, both B and C - are enabled, multiplexors D and E are selecting the other inputs, MDØ 00-15. At the same time, the output buffer H is put in the high impedance state. Although MDI 8-15 is gated back from G to E and Data In (DIB 8-15) is enabled by multiplexor B, they have no effect since D and E are always selecting the MDØ inputs during read cycles. Output multiplexor J selects Bus 0-7 (via ERCH being low) to gate to BIO 8-15N.

SIGNAL NAME	RW	WW	RLC	RRC	WLC 1	WLC 2	WRC 1	WRC 2
RSLN (PWUP)	H when normal power available →							
RSL	L when normal power available →							
TMRN (MRN)	L when master requests read/write memory cycle →							
TMR	H when master requests read/write memory cycle →							
CASEL/ADSEL	H if address recognised on this PCB							
MAD 15	*	*	L	H	L	L	H	H
CHA (CHAV)	L	L	H	H	H	H	H	H
CHAN	H	H	L	L	L	L	L	L
WRITE (WRITEV)	L	H	L	L	H	H	H	H
READ	H	L	H	H	L	L	L	L
ERCH	H	H	L	H	L	L	H	H
ELCH	H	H	H	L	H	H	L	L
ERCHN	L	L	H	L	H	H	L	L
ELCHN	L	L	L	H	L	L	H	H
RDCY	L	L	L	L	H	L	H	L
MCY	H	H	H	H	L	H	L	H
WCY	L	H	L	L	L	H	L	H
RWDS	H	L	H	H	H	L	H	L
DCYN	H	H	H	H	L	H	L	H
RCY	H	L	H	H	L	L	L	L
SFN	— * — L if read error					* →		*
RFRON/RFCYN	H during the time when TMRN is L →							
CLLAT (at time T6)	L	L	L	L	H	L	H	L
TRDØLN	L	H	H	H	H	H	H	H
TRDØRN	L	H	L	L	H	H	H	H

SYMBOLOGY -

RW	Read Word Cycle	1	Read part of WLC or WRC cycle
WW	Write Word Cycle	2	Write part of WLC or WRC cycle
RLC	Read Left Character Cycle	*	Don't care
RRC	Read Right Character Cycle	H	Logical '1' level
WLC	Write Left Character Cycle	L	Logical '0' level
WRC	Write Right Character Cycle		

Table 6.1 DATA TRANSFER SIGNALS

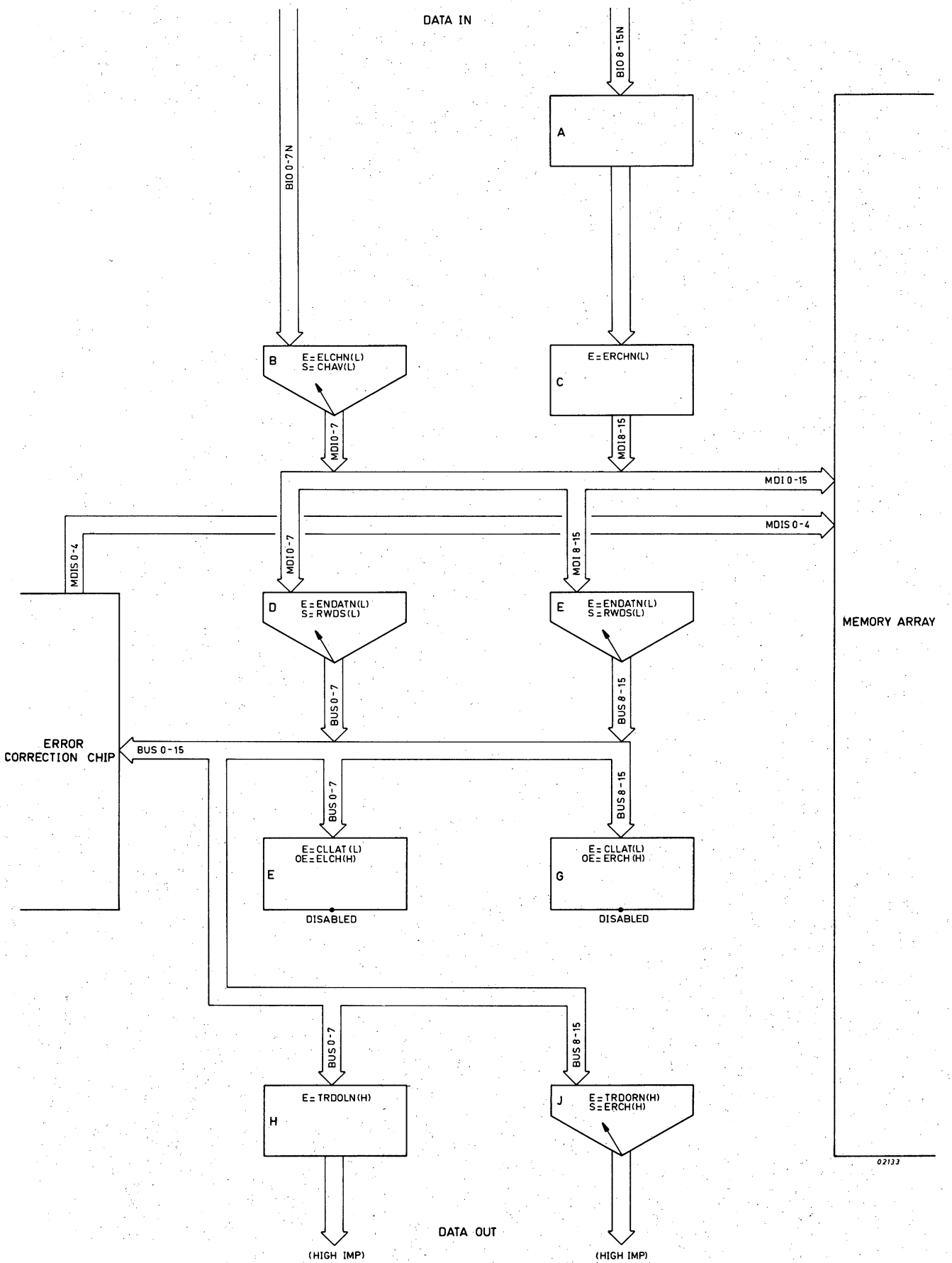


Figure 6.1 WRITE WORD

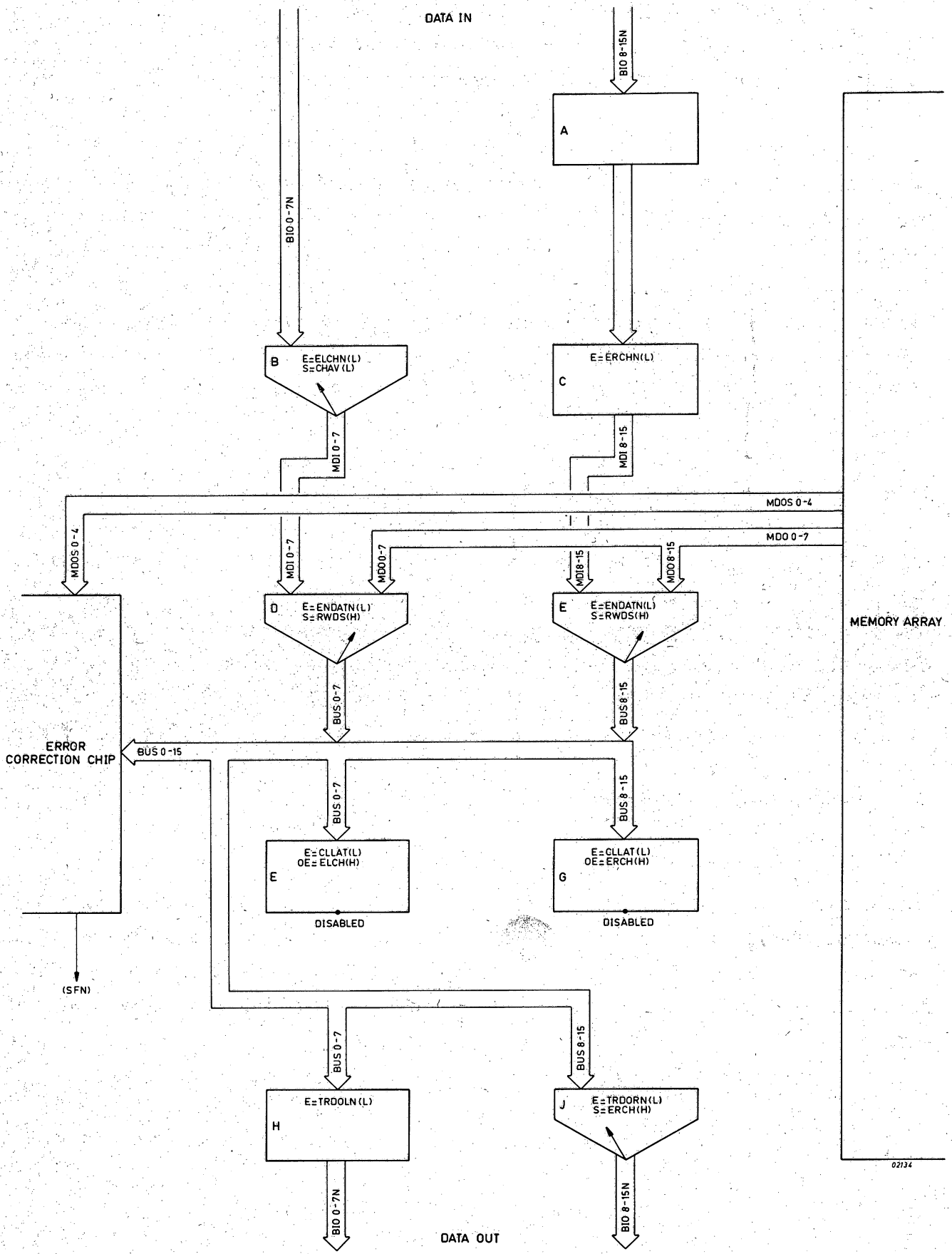


Figure 6.2 READ WORD

d) READ RIGHT CHARACTER - See figure 6.4

This is similar to Read Left Character except that ELCH is now low and ERCH high so the right character, BUS 8-15, is selected and gated to BIO 8-15N.

e) WRITE LEFT CHARACTER - See figure 6.5

The Write Character cycles are rather more complicated, requiring as they do part of the memory word being retained and re-written, together with the new character. This requires two successive memory cycles, the first to read a word from the desired address and, if necessary, correct it, and the second to select the desired "new" character and the opposite "old" character and write them back into the same location as a word. During the "read cycle", the word is read out of the array as MDØ 00-15 and MDØS 0-4 and is gated to the ECC by RWDS being high.

If necessary the word is corrected. During this cycle, latch F is disabled by ELCH being H latch G is enabled by ERCH being low while CLLAT is high (gating BUS 8-15 back to the, at this moment, unselected input of multiplexor E as MDI 8-15). Multiplex B then selects BIO 8-15N (the "new" character) and gates it to the unselected input of multiplexor D as MDI 0-7. When the "Write cycle" begins CLLAT latches BUS 8-15 into latch G and RWDS going low selects the other inputs of multiplexors D and E to gate MDI 0-15 to the ECC. The ECC forms the error correction bits from the 16 data bits and so MDI 0-15 and MDIS 0-4 are written into the selected address. Buffer C, latch F and the output drivers H and J are all disabled throughout this double cycle.

f) WRITE RIGHT CHARACTER - See figure 6.6

This cycle is nearly identical to the Write Left Character cycle with the exception that multiplexor B and latch G are now disabled such that MDI 0-7 is the corrected output from the read cycle and MDI 8-15 is gated from BIO 8-15N. As in the WLC cycle, the output drivers H and J are put into the high impedance mode.

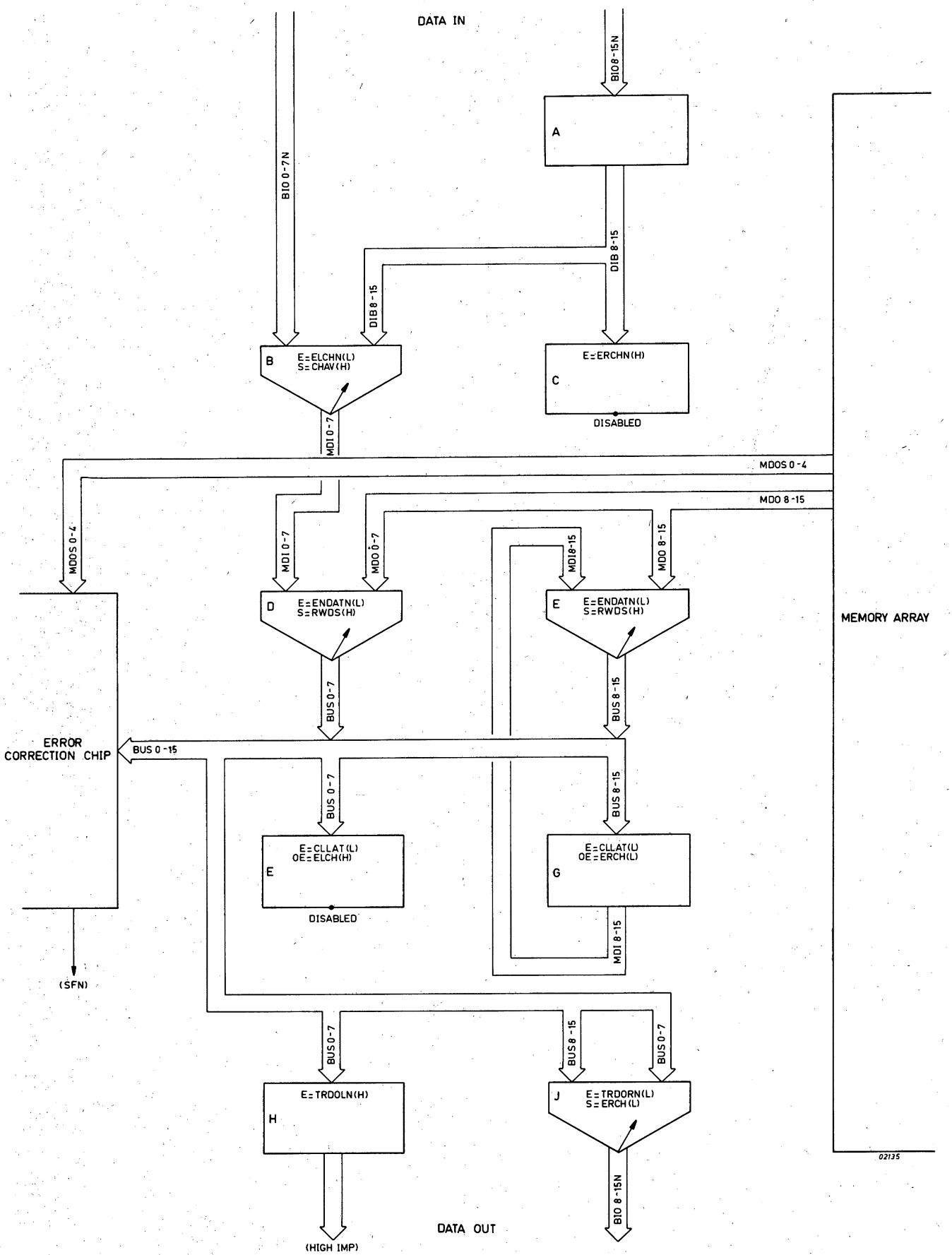


Figure 6.3 READ LEFT CHARACTER

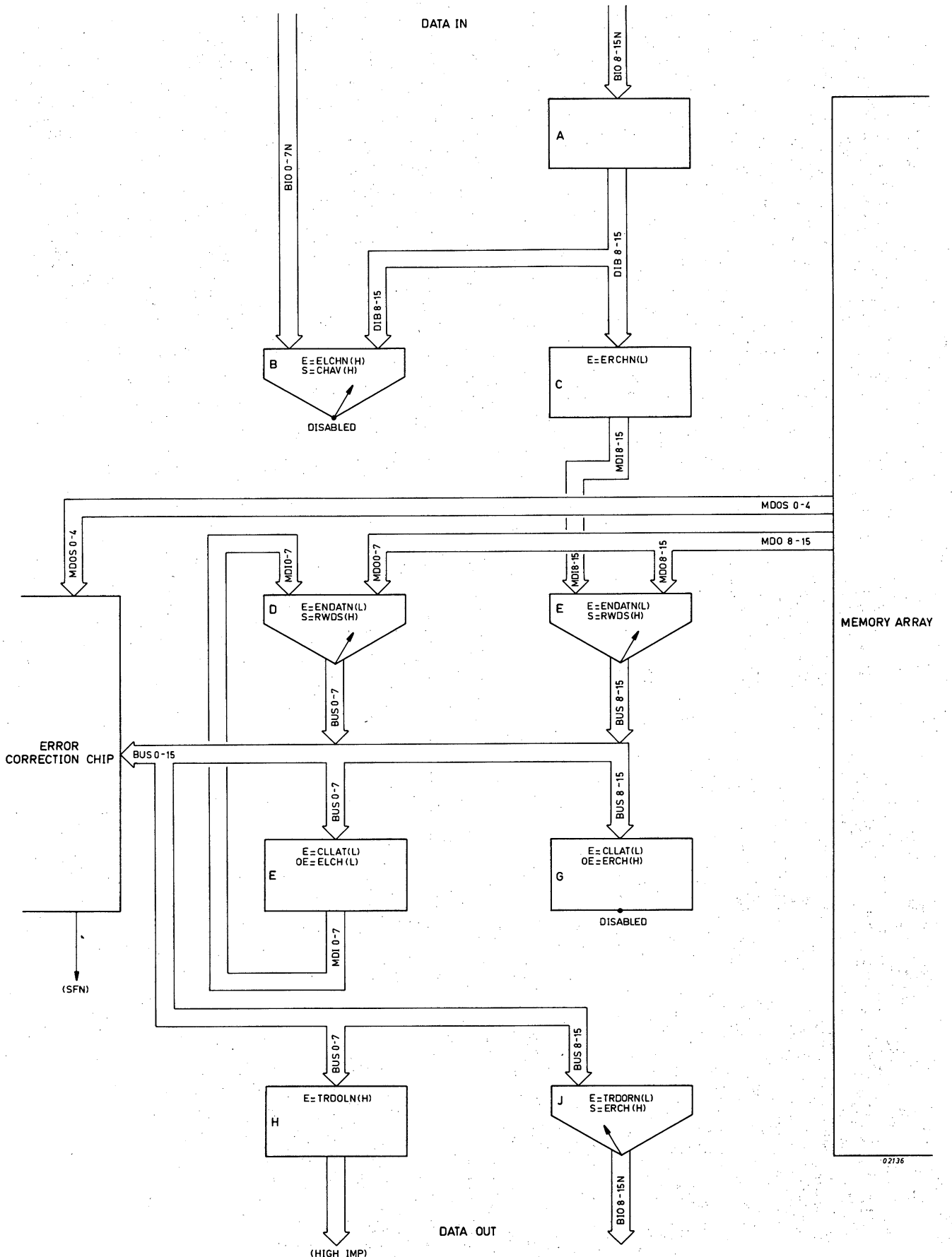


Figure 6.4 READ RIGHT CHARACTER

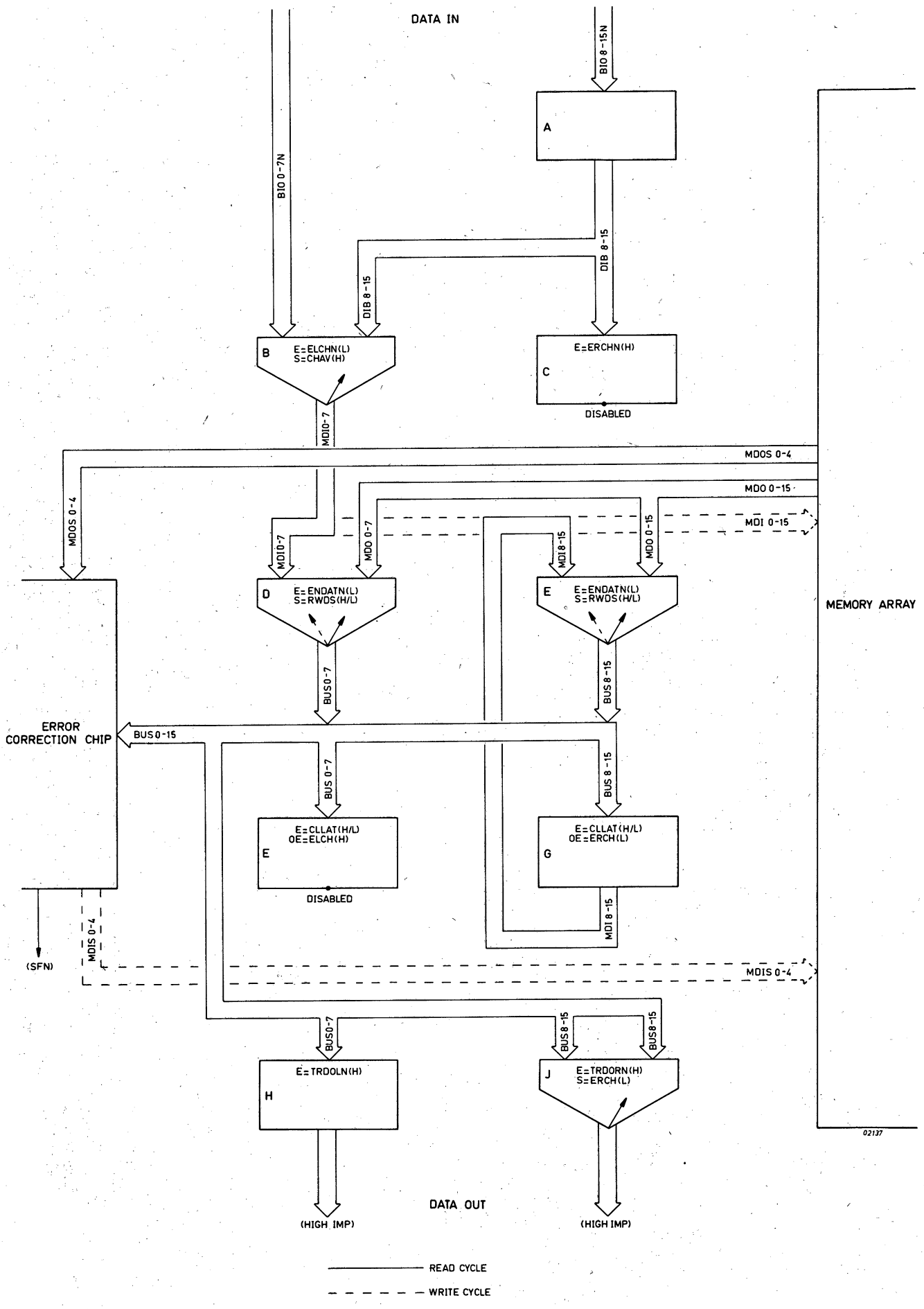


Figure 6.5 WRITE LEFT CHARACTER

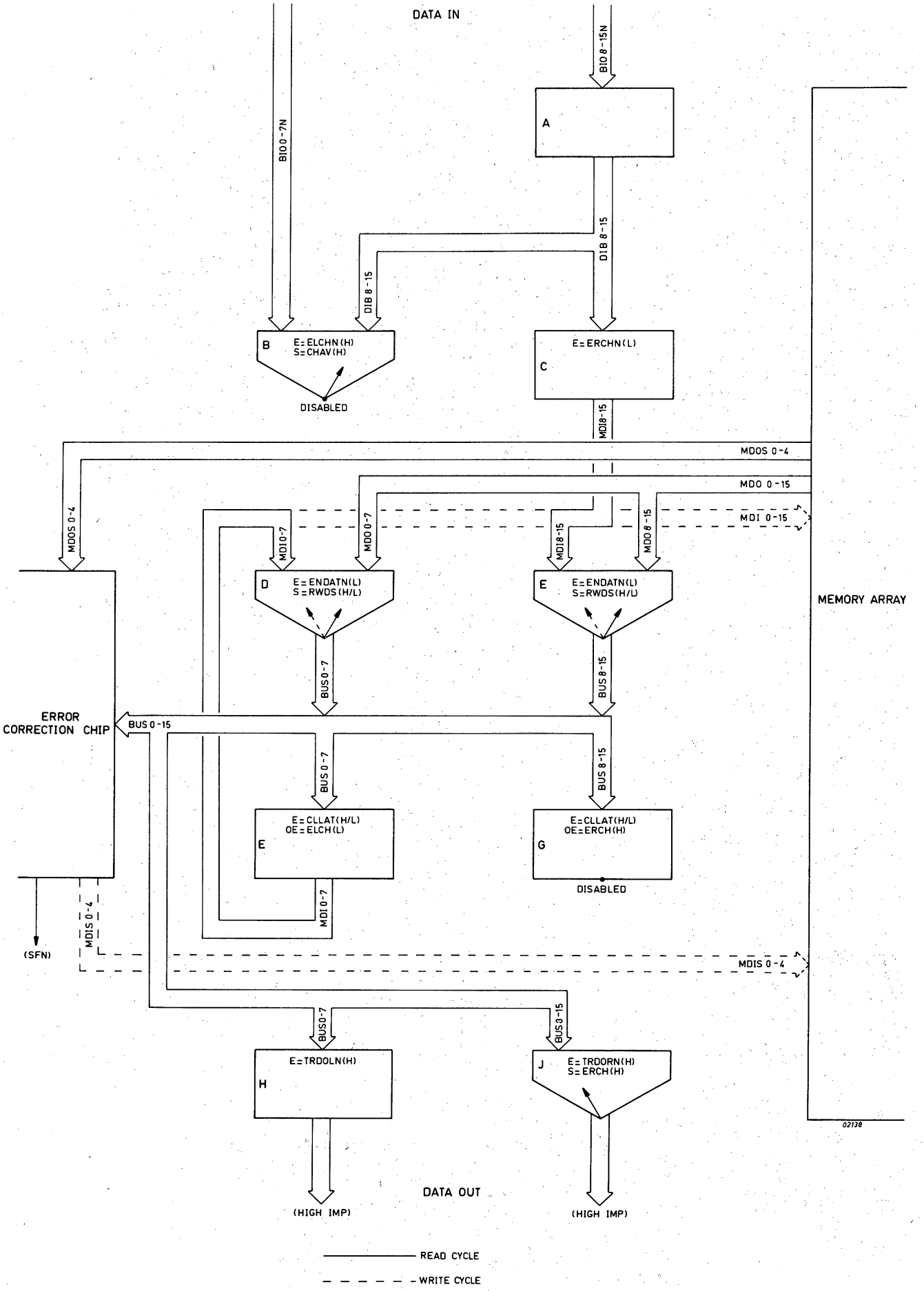


Figure 6.6 WRITE RIGHT CHARACTER

6.2 MEMORY ARRAY

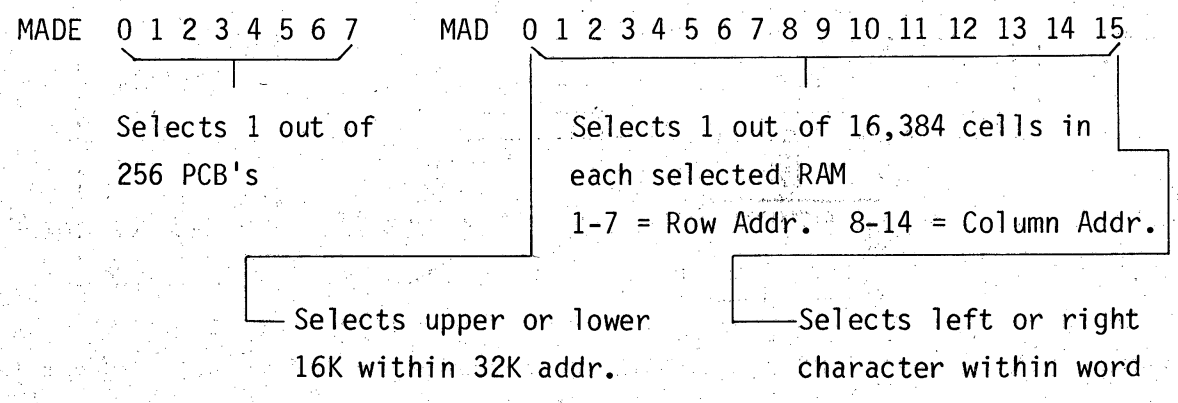
As mentioned previously, the WMA-1 PCB is optionally available in either 16K or 32K word capacities, although mainly the latter version is intended for the P4500. Therefore, in the following diagrams, the full configuration is illustrated.

The RAM chips have a capacity of 16K bits and the word size is 16 bits + 5 error correction bits so that 21 RAM's are required to enable a 16K word to be addressed, (the 32K PCB, therefore, contains 42 RAM chips).

The 7 address lines (A0-A7) are presented to all the RAM's, as is the read/write mode signal WEN (Write Enable - derived from WRITE). As can be seen from diagram 1 - Memory Array, the RAM's are arranged in four "bars" on the PCB, two of which contain the lower 16K (0-16K) and two of which contain the upper 16K (16-32K), if present. The lower 16K is strobed by RASON while the upper 16K is strobed by RAS1N (or is not available in a 16K PCB - see Address Selection). All four columns are strobed by signals CASN(0-3) which are all derived from CAS. Thus the Column Address is strobed into all the RAM's by CAS but the Row Address is only strobed into the selected 16K. Also, in each "half" of the array (ie., upper and lower 16K) each RAM handles only one bit of each word stored in the memory. Thus one individual RAM is responsible for bit 0 for the whole 16K and so the data in pin is connected to MDI00 and the data out pin to MDØ00.

6.3 ADDRESS SELECTION

There is a total of 24 bits used for the address selection, organised as follows:



Examples of several address selections are shown in chapter 3 - Strap Setting.

Referring to diagram 1 - Address Selection, MAD (Memory Address) bits 1-14 are fed into seven multiplexors such that when one set of inputs is selected, bits 1-7 are gated through and when the other set of inputs is selected, bits 8-14 are gated through. This set of multiplexors is enabled whenever a refresh cycle is not taking place and the input selection is by the signal MX from the Timing (see Timing Read/Write Cycle). The MAD signals are gated through a set of 'OR' gates (whose other inputs derive from the Refresh Address Counter) to produce the address signals A(0-6) which are presented directly to the memory array.

The MADE (Memory Address Extension) bits, together with MAD00, are presented to nine latches and latched in as MRN (derived from TMRN when a Master makes a request) goes low. The output of each latch is the respective MADE or MAD00 signal and its complement. In each case, either the signal or its complement is selected by a strap (see chapter - Strap Setting). The signal enabled by the Strap for MAD00 is only used for 16K modules, otherwise it is strapped to be permanently high for 32K modules. The nine "outputs" of the straps, ADSE(0-7) and ADSEL are ANDed to form the signal EXT (Extension) when all the outputs are high. EXT is also strapped to form CASEL (Card Select) if more than one card is present in the memory. Otherwise, if only one card is present, the address extension is not needed and CASEL is strapped permanently high.

This address extension facility is provided so that when there is more than one memory PCB in the system, each PCB can be allotted a unique extension address to identify it from all the other PCB's in the system. (The exception to this is that two 16K PCB's may be present and are selected by MAD00). Thus, the extension straps are set up in such a way as to strap the high signals (ADLE0-7 or their inversions) to enable CASEL on only one PCB. MAD00 is only used to identify upper or lower 16K on a 32K PCB but is used as part of the address extension with 16K PCB's. The various combinations of MADE and MAD00 are illustrated fully in chapter 3 - Strap Setting.

Signals CASEL (Card Select) and ADSEL (Address Select) are used to enable the memory cycle when high and disable it if low (see Timing Read/Write Cycle).

In a 16K PCB, signal AD00 is strapped permanently low to enable RASON (which strobes 0-16K) for every operation. While MAD00 is low, RAS1N (16-32K) is disabled, but while MAD00 is high, RAS1N is enabled as well as RASON. This has no effect, however, as there are no RAM's present on the array to be strobed by RAS1N.

A mention will also be made here to the Refresh Address Counter which provides a 7-bit row address during a refresh cycle (see Timing Refresh Cycle). It consists of two 4-bit counters in cascade - that is effectively an 8-bit counter counting to 256 (actually 0 to 255). During refresh, we must select one of the 128 rows in each RAM so the MSB of this counter is not used and it effectively counts from 0-127.

The counter is never cleared (because LT is continuously low since the initial state of the counter is totally irrelevant) and is clocked by the signal RFCY, indicating that a refresh cycle is taking place. As the counters clock on the H⟶L clock transition, the Refresh Address Counter increments by one at the end of each refresh. The outputs of the counter, RAC(0-6), are ORed twice, once with the signal ARFCYN and once with the normal read/write address signals, ADM(0-6). The first OR disables the RAC during a read/write memory access while ARFCYN is high and inverts RAC(0-6) during a refresh, when ADM(0-6) are all low (because ARFCY is high during refresh) thus gating the RAC outputs to the A(0-6) signals.

The previous paragraphs have described how A(0-6), RAS0/1N and WEN are presented to the memory array. Since data in and data out will be described later, it only remains to discover how CASN(0-3) are formed. The signal CAS, like RAS, comes from the Timing Read/Write Cycle section. These signals are active high and become active at certain fixed times within the memory cycle, whether it be a read, write or refresh cycle.

During a read/write cycle, RFCYNV is high so at the moment CAS goes high then all four signals CASN(0-3) all go low to strobe the column address into all the RAM's on the card (four NAND gates are used because of the load). During refresh, RFCYNV is low and disables the CASN(0-3) signals. These remain inactive (high) to indicate a refresh action to the RAM's.

6.4 ERROR CORRECTION CIRCUITRY

The error correction circuitry (encoding, decoding and correction) for the WMA-1 memory has been incorporated into a single 40 pin LSI chip. The ECC works, internally, in a very similar way to the MSI circuitry of the KMA-1 memory, the exceptions being that a fifth error correction bit is necessary because of the 16 bit word and the parity encoding and decoding is done by the same logic. Figure 6.7 shows a simplified block diagram for the ECC. Note that some of the features of the chip, such as double error detection, are not used.

During a write cycle, the 16 data bits are presented to the bi-directional Bus and clocked in with CLEC (Clock Error Correction) and latched (CL1 clocks data bits 0-7 and CL2 clocks data bits 8-15 and the S bits). The five 'S' bits are formed by encoding five combinations of certain data bits and are eventually driven from the output buffer to the memory array by BUSEC (Bus Error Correction) going low (the data bits are also driven at this time).

During a read cycle, the 16 data bits and five error correction bits from the memory are clocked into the input buffer and decoded. Note that the signal on ENCH (Read/Write Data Select) decides whether an encoding (ENCH is low) or decoding (ENCH is high) is required. RWDS is held high for read word/character and also the read part of write character. If there is no error, the Error Decoder stage of the ECC sets SFN (Single Failure Not) high (inactive) and the data is driven out of the output buffer by BUSEC. If an error is detected, SFN is set low to indicate an error, the error is corrected and the corrected data driven out by BUSEC.

Although the facility for double error detection is built into the ECC it is disabled by SEDE being held high. Thus a single error will be corrected user-transparently but a double error is completely undetected and incorrect data driven onto the Bus.
Diagram 2 shows the logic diagram of the ECC.

6.5 DATA IN/OUT

The data interface between the memory and the other system elements is via the 16 data lines BIO(00-15)N. The bits 0-7 are only used during word transfers. Reference diagram 2 DATA IN and DATA OUT.

During a memory write cycle, data is presented to an input buffer consisting of three elements (two buffers and a multiplexor). The right-hand character is presented to the first buffer from which it goes to both the other elements. The buffer dealing with bits 8-15 is enabled during write word and write right character operations while the multiplexor dealing with bits 0-7 is enabled for write word (when it selects BIO 0-7N) and write left character (when it selects DIB 8-15, the output of the first buffer) operations. The output of this stage is gated, as MDI 0-15, to both the memory array and to another set of multiplexors which enable MDI 0-15 to the Error Correction Chip. The outputs of the ECC are the data bits BUS 0-15 and the error correction bits BUSS0-4.

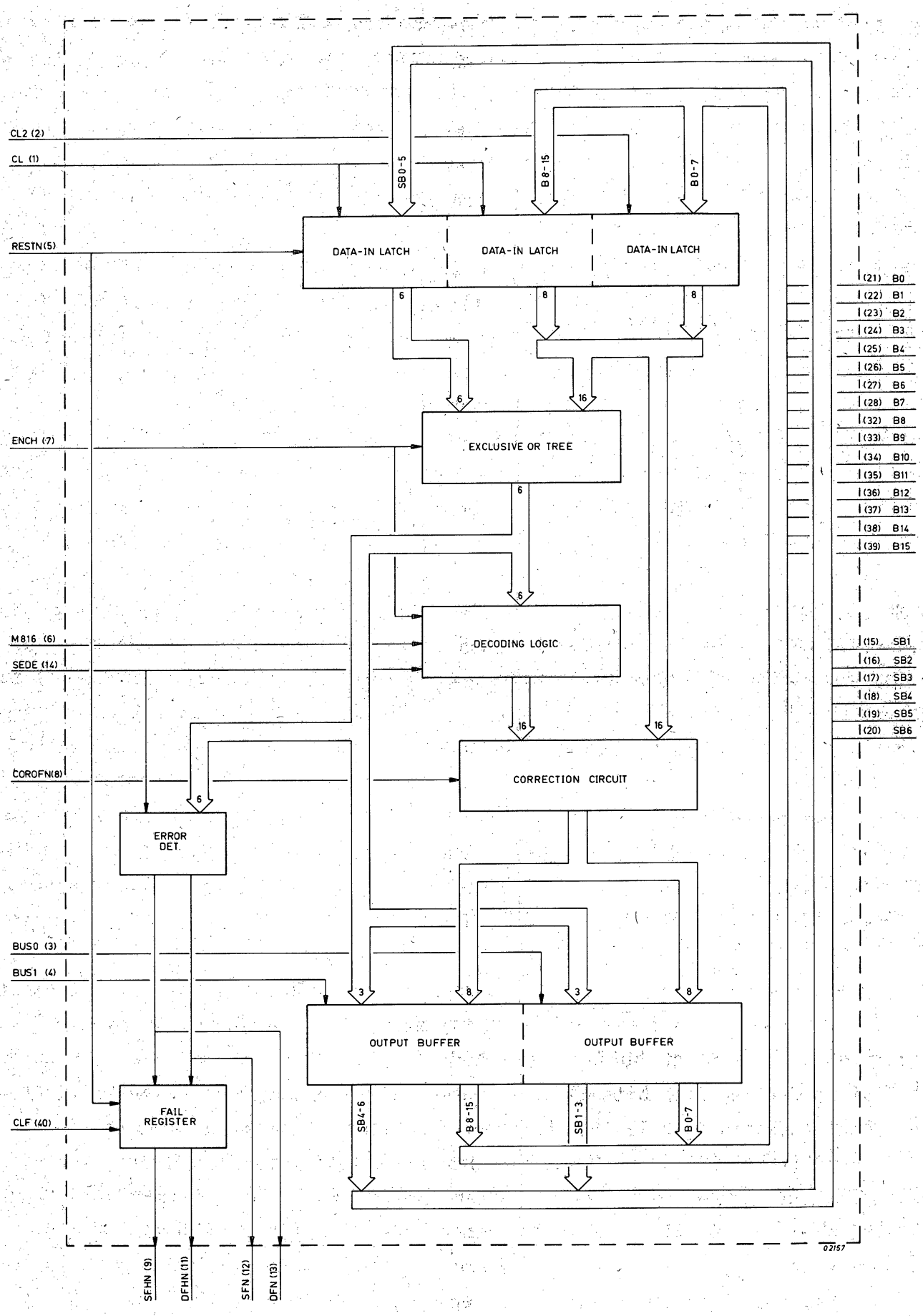


Figure 6.7 SIMPLIFIED BLOCK DIAGRAM - ERROR CORRECTION CHIP

For a write word, BUS 0-15 are not required but BUSS0-4 are driven through a multiplexor, which is only used for diagnostic purposes, to the memory array as MDIS 0-4. These error correction signals are produced in the same way for a write character but now the BUS 0-15 signals are also used. During the read part of a write character double cycle, the word is read out of memory, corrected, if necessary, and then driven out of the ECC by BUSEC. During a character operation, one or other of the latches F and G are enabled (F for a right character) and the enabled latch allows the required character of "old" data to be gated back to the multiplexors D or E (ie., in a write right character operation, the "old" left character is gated back to multiplexor D by latch F).

The write cycle may now begin with multiplexor D gating the "old" left character (MDI 0-7) and multiplexor E gating the "new" right-character (MDI 8-15 via input buffers A and C) to the ECC. Thus the new 'S' bits are produced and written back to the memory array, along with the data bits, strobed by the signal WEN.

During a memory read cycle, the complete word is read out of the array as MDØ 0-15 and gated through multiplexors D and E to the ECC for checking and possible correction. The data, as BUS 0-15, is also presented to latches F and G and to the output buffer H and J. F and G are enabled during character cycles but are only useful during write character operations. During read character cycles, one or other of the latches is enabled and gates one or other character back to the inputs of multiplexor D or E. During read cycles, these multiplexors are always selecting MDØ and not MDI. As previously mentioned, as soon as the data out is gated through to the ECC it is also presented to the output drivers (multiplexor J and buffer H). These are enabled very soon afterwards to drive the data onto the BIO lines, even before it is corrected.

If there is no error, the ECC takes over driving the data, as BUS 0-15, onto BIO 00-15N or, if there is an eror, the corrected data is now forced by the ECC. There is a slight overlap between the driving of the ECC and the switching off of the multiplexors D and E which will be described under Timing Read/Write Cycle. Note that only for a read word will both output drivers be enabled - for read character operations only multiplexor J is enabled and, depending upon whether the left or right character is required, it selects either BUS 0-7 or Bus 8-15.

The 'S' bits, when read from memory, are first presented to multiplexors (which are enabled by the same signal and at the same time as multiplexors D and E for the data bits). These select MDØS 0-4 during normal read cycles, and the read part of write character cycles, but select low inputs for all other cases.

6.6 TIMING READ/WRITE CYCLE

a) GENERAL

The timing for all the various memory cycles, including refresh, is centered upon a shift register, part of which consists of a 4-bit serial-or-parallel-input shift register device and part of which consists of four flipflops so arranged as to form a second 4-bit Shift register (with both direct or inverted outputs). The shift register, as a whole, provides the RAS, and CAS pulses which strobe the seven-bit row and column addresses into the RAM's (see Address Section and Memory Array).

The clock signal for the shift register and other devices in the timing logic is provided by a 16MHz oscillator which provides signals CL and CLN to the logic at 62.5ns periods.

The shift register itself is a 4-bit device which, in the WMA-1 memory, may be used in serial-input shift-right mode or parallel input mode. In the former mode, the signal on the Data Shift Right input is transferred to the first output, Q0, on the low-to-high transition of the clock signal, CL. At the same time, the previous contents of Q0 is clocked to Q1 and so on. In the parallel input mode, the signals on the inputs P0-3 are transferred to the respective outputs.

With reference to Figure 6.8 - Main Cycle Timing, it can be seen that the initial state of the counter is serial input mode with the signal on the Data Shift Right input, CYREQ (Cycle Request), being low. This means that until CYREQ goes high, none of the outputs is active. CYREQ, as will be seen later, is activated either by the refresh logic or a read/write request by a master via TMRN.

On the next clock following the activation of CYREQ, output QO goes high, activating the RAS signal. The address will already be presented to the address multiplexors and the row address (bits 1-7) selected, so the RAS signal (Row Address Strobe) will strobe the row address into one of the 16K parts of the memory array. One clock later the signal MX (Multiplexor) selects address inputs MAD 8-13 at the address selection multiplexors and, one clock later still, CAS strobes this column address into every RAM on the card. At this point the RAM's begin their own internal cycle to read, write or refresh.

Meanwhile, CYREQ is still high so RAS and CAS remain active while, during successive clock periods, T3 and (through D-type flip-flops) T4, T5, T6 and T7 become active (high). However, the shift register changes its mode now depending upon whether there is an error or not in a read cycle. In a write cycle, a refresh cycle, or a read cycle in which good (ie., correct) data is read, the shift register changes to parallel input mode at time T6 (as T6N goes low). At this moment both T3 and RAS outputs are high so, one clock later, they are fed back to the parallel inputs, together with a low signal on P4, to force the outputs QO-3 into the state HHHL. This means that T3 goes low again at time T7.

One clock later, still in parallel input mode, RAS goes low because its input, T3, is also now low and, because RAS goes low, MX and CAS both go low one clock later still (ie., time T9). However, when T3 goes low, it effects the series of D-type flip-flops with the result that T4, T5, T6, and T7 fall at consequetive clocks after T3. At the time that T6 goes low, the mode of the shift register reverts to serial input (at time T10) and so it is possible to begin another memory cycle on the upward (low to high) transition of the following clock, CL, at time T11.

If, however, an error was detected during a read operation, the cycle is extended slightly to allow for correction. Signal T7ERN becomes active (low) and prevents the shift register from reverting to serial input mode until T7 goes low, which is one clock later than in the "short" cycle. This also delays the earliest time at which a new memory cycle may begin until T12.

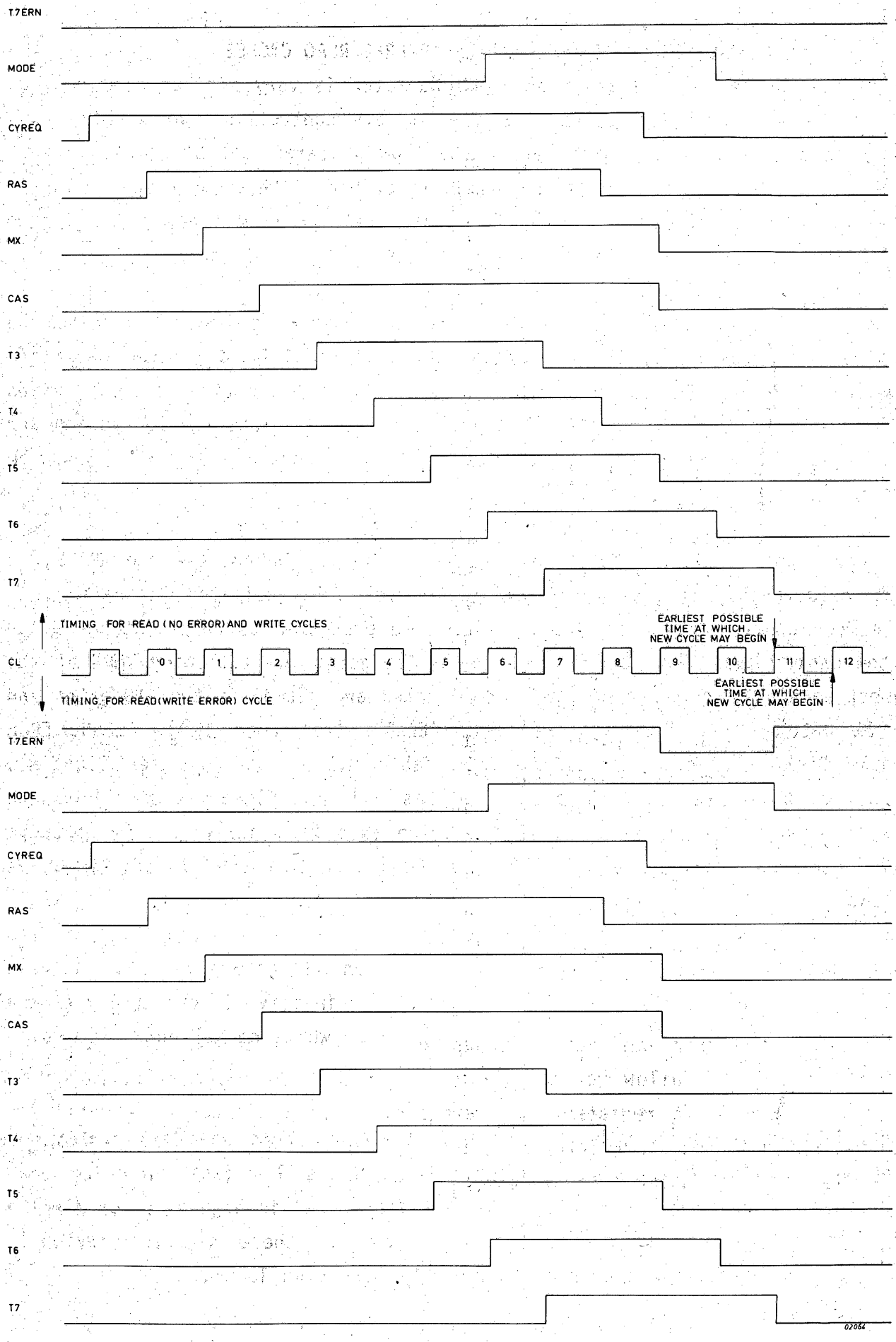


Figure 6.8 MAIN CYCLE TIMING

b) TIMING FOR WRITE WORD AND ERROR-FREE READ CYCLES

The timing for write word and read word/character is very similar, the ovvious main difference being of course, in the signals controlling the enabling and selection of the devices which handle the flow of data. All these variations use the "short" cycle timing as previously described if there is no error in the read. The following description is made with reference to diagram 3 - Timing Read/Write Cycle A and B.

Prior to a master activating the TMRN (Timing Master to Memory) signal, the address lines MAD 00-15, the address extension lines MADE 0-7, the read/write and word/character mode signals and, if it is a write operation, the data in on BIO(00-15)N, must all have been previously activated. Since the addressing and data signals have been described elsewhere, the mode control signals will now be described.

The three mode control signals are, at the interface, MAD15, CHA and WRITE and their relationship to the various possible cycles is indicated in Table 1.1 - Cycle Mode Control Signals. These signals are presented to three latches prior to the memory cycle and are latched in by MRN going low following TMRN at the request time. The outputs of the three latches are gated via two AND gates and two OR gates to form the signals ELCH (Enable Left Character), ELCHN, ERCH (Enable Right Character) and ERCHN (see Table 6.1 - Data Transfer Signals), which enable and select the various latches and multiplexors controlling the data flow which the different cycles require (see Data In/Out). The outputs CHAV (Character Mode), CHAV, WRITEV and READ are further used in the timing as follows.

Signal RCY (Read Cycle) is activated (high) by an AND gate if RFCYNV (Refresh Cycle Not), Read and PWUP are all high. RFCYNV is inactive (high) at any time a refresh is not taking place, PWUP is active (high) while normal power is available and READ is high if WRITE is low.

Signal MCY is permanently high throughout the Write Word and Read cycles now being described because RDCY (Read Double Cycle) is low (see following description of Write Character). Signal WCY (Write Cycle) is high only for a Write Word Cycle (also during Write Character) and all these signals previously mentioned are used elsewhere in the timing, as described later.

Signal RWDS is high during the read cycles to put the Error Correction Chip in "decode" mode (see Error Correction Chip) and low during Write Word for "encode" mode. It also selects MDØ or MDI at multiplexors D and E depending upon whether a read or a write is taking place. CLLAT (Clock Latch) is low during Read and Write Word cycles to keep the latched F and G latched (see Data In/Out).

With normal power on the memory, signal RSLN (Reset Line Not) is high. This signal is inverted twice by buffer inverters to form RSL (normally low), and PWUP (Power Up - normally high). Similarly TMRN is inverted by identical elements such that when TMRN goes low (indicating a request by a master) TMR goes high and MRN (Memory Request Not) goes low.

The first gate in the sequence to start up the shift register is a three input AND which disallows the request if there is a power failure (via PWUP), or if there is a request for a refresh cycle (RFRQN - Refresh Request Not). If all three are high then ENREQ (Enable Request) goes high and, at next positive transition of the clock, CL, MREQ (Memory Request) also goes high. (This sequence of events may also be followed on figure 6.10 - Read Word - No Error).

MREQ is one of four inputs to a NAND whose other inputs are TMR, CASEL and ADSEL. TMR is derived from TMRN as described above and CASEL (Card Select) and ADSEL (Address Select) are high if this particular memory card is selected by the address extension signals and bridges (see Address Section). If all these inputs are high then RWCYN (Read Write Cycle Not) goes low (active). This is one of four inputs to another NAND, any one of which going low forces the output CYREQ to go high and thus begin the shift register cycle. At this moment, the other inputs to this NAND are all high (there is no refresh cycle taking place and RAS, at this moment, is low forcing CYBUSYNV low). On the following clock, however, the shift register cycle forces RAS high so CYBUSYN (Cycle Busy Not) and CYBUSYNV both go low (though this has no effect with this cycle).

Thus the shift register starts up as previously described and the signals RAS, MX, CAS, T3, T4, T5, T6, and T7 appear in succession. As RAS goes high, it forces signal RBUSECN (Reset BUSEC Not) low as the other inputs of the NAND gate, RFCYNV and MXN, are at this moment both high also. As RBUSECN goes low it resets the three D-type flip-flops controlling the signals CLEC (Clock Error Correction), BUSEC (Bus Error Correction) and ENDATN (Enable Data Not). Thus ENDATN goes low to enable the multiplexors D and E (see Data In/Out) to drive either MDØ (for a read) or MDI (for a write) to the output drivers and the ECC.

At the same time CLEC goes high (transparent mode) to enable the data on BUS 0-15 (and BUSS 0-4, if a read cycle) into the input buffer of the ECC (see Error Correction Chip) and BUSEC goes high (high impedance state) to stop driving the previous data (from the output buffer in the ECC of the previous read/write cycle) out onto the Bus lines.

One clock after RAS, MX goes high to select the column address inputs (see Address Selection), reset RBUSECN high (to enable all the flip-flops) and, in the case of Write Word, to activate (low) WCLECN (Write Clock Error Correction Not). WCLECN is one of four inputs to a NAND gate, the output of which goes high if any of the inputs goes low. Thus ENCLEC (Enable CLEC) goes high and, at the next clock CL, CLEC goes low to latch the data in the input buffer of the ECC. During a Read cycle, WCLECN remains high and RCLECN (Read Clock Error Correction Not) does not go low until time T5 (due to RCY and T5 inputs to a NAND) and it is not until one clock later that CLEC goes low (this is because the data is not available from the RAM's until some time after CAS).

CLEC going low effects the input of the next flip-flop and so, one clock later, BUSEC goes low to drive the data in the output buffer of the ECC onto the Bus lines. ENDATSN (Enable Data 'S' Not - the error correction bits) which has been driving the error correction bits from the 'S' Data Out Multiplexors (see diagram 2 - Data Out) is made high at this time, putting the multiplexors in the high impedence mode. In a Write Word cycle, ENDATN goes high (inactive - high impedance mode) at the same time as BUSEC (ie., one clock after CLEC goes low) due to WENDAT (Write Enable Data) going high (an NAND gate with WCLEC, the inverse of WCLECN, and CLECN as inputs, both now high) forcing DENDAT (D Enable Data) and, one clock later, ENDATN high (into the three state mode). In the read mode, ENDATN goes high one clock after BUSEC, due to WENDAT remaining high and ENDATN requiring one extra clock now.

The outcome of all this is that, during a read cycle, data is available from the memory array some time after CAS goes high. (Refer to Figure 6.9 - Read Word No Error). At time T6 (one clock after T5) CLEC goes low to latch the data in the ECC input buffer and begin the parity decode. At the same time, this data on the BUS is being driven by multiplexors D and E to the output buffers H and J.

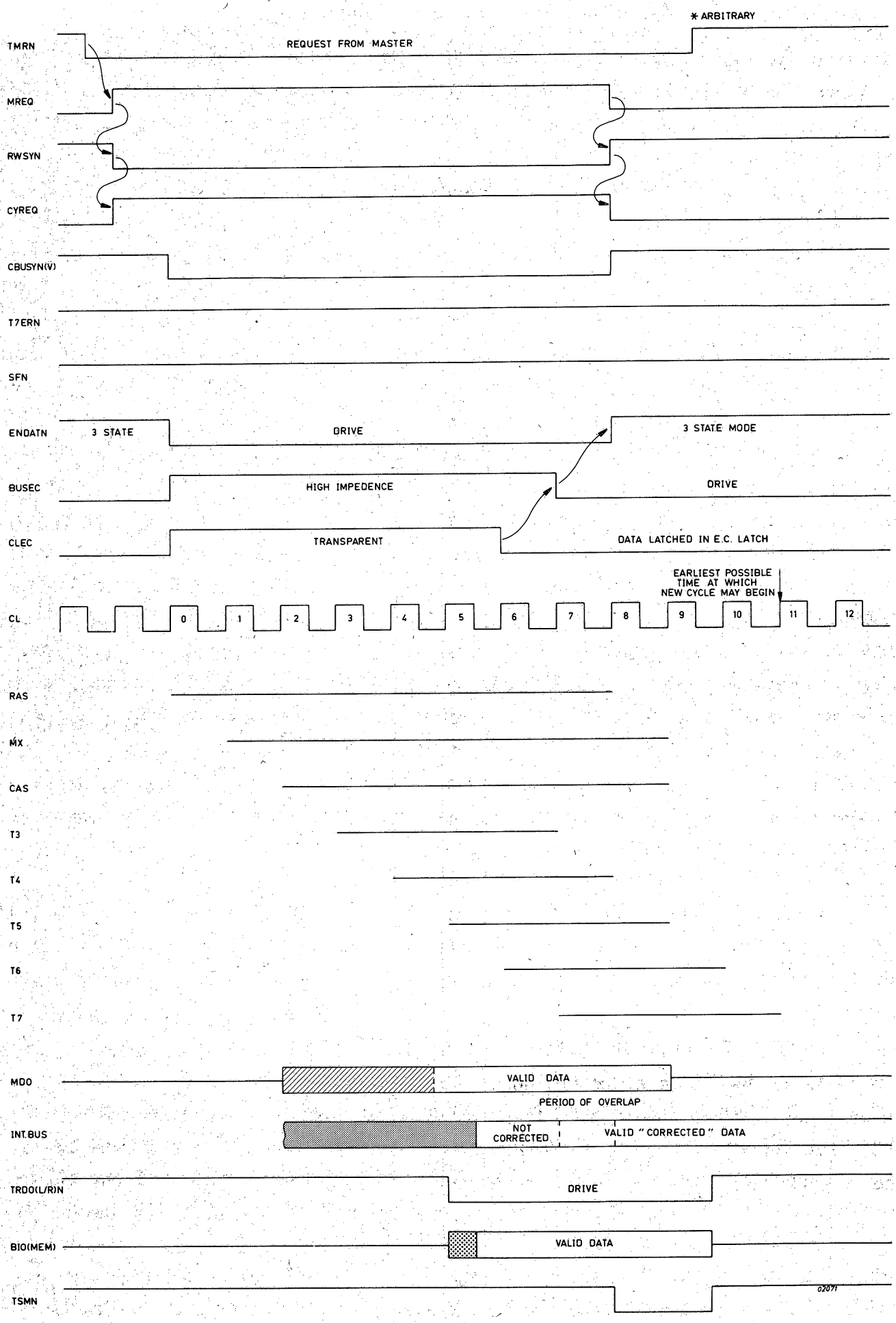


Figure 6.9 READ WORD - NO ERROR

Whatever the cycle (Read Word or Read Character), the multiplexor J is enabled by TRDØRN (Transmit Data Out Right Not). This comes about because RCY is high during a read cycle and, if ADSEL and CASEL (from Address Selection) are high, then ENTRDØ (Enable Transmit Data Out) goes high and at time T5 (as T5N goes high to low) a JK flip-flop enables TRDØ. TRDØ and TMR (still high from TMRN) enable TRDØRN to go low and drive the data onto the BIO lines (at this moment this is uncorrected data). TRDØLN is enabled for Read Word cycles by CHAN being high (word mode).

So for a short period of time, uncorrected data is being driven on the Bus lines by multiplexors D and E and then onto the BIO lines by TRDØRN (and possibly TRDOLN if Read Word). But at time T7, BUSEC drives the output buffer of the ECC onto the Bus while the multiplexors D and E are still driving. D and E do not switch off until one clock later with ENDATN, so for a short period (something less than a clock cycle) there are two sets of drivers forcing data onto the Bus. If there is no error in the data this is no problem as they are both driving the same data, (see paragraph 3 for read cycles with error description). Thus when ENDATN disables the multiplexors, BUSEC is left driving correct data onto the Bus and will continue to do so until the beginning of the next read/write cycle (a refresh is internal to the RAM's as far as data goes so that data out from the previous cycle is still available on the Bus until the next cycle).

During a Write Word, TRDØ (L/R)N are disabled because RCY is low and the outputs of the buffer H and J remain high impedance. There is a strap to indicate whether the WMA-1 is being used:

1) in a P4500 System in FSM mode,
2) in a P4500 System in P851 mode or
3) in a P851 System

For the latter two cases see "P851 Mode". For the P4500 in FSM mode it means that signal FSM is high and P851M is low (see Strap Setting). This is mentioned because it effects the formation of signal TSMN (Transmit Slave to Master). For a Write Word Cycle, WCY (high during a write) and T78 (formed when T4, T7 and FSM are all high - ie., at time T7) are presented to an 11-input AND-OR-NOT device. This is effectively four AND gates (one 4-input, one 3-input and two 2-input) with each output going to a 4-input NAND. In other words, if any of the combinations on the AND inputs are all high then the output of the device is low. Thus with WCY and T78 both high, ENØK (Enable OK) goes low and, one clock later (at T8) ØK goes high and ØKN goes low. As TMR is still high, ØK now enables TSMN to go low, indicating to the master that data has been successfully written into the memory.

During a read cycle without error, ENØK is enabled by the combination RCY, SFN (high if no error) and T78. Of the other two AND functions, one is dealt with in paragraph c - Read With Error, and the other is described in "P851 Mode".

As ØK goes high and enables TSMN, ØKN goes low and holds the flip-flop in the reset state. ØKN is also fed back to a D-type flip-flop right at the beginning of the timing logic and resets MREQ, at the same time blocking any further requests. By this time, the shift register is already in parallel input mode so CYREQ may now be dropped.

All is now waiting for the master to respond to TSMN by making TMRN inactive (high) again. When this happens, the drivers TRDØRN (and also possibly TRDØLN, if in use) are disabled, the ØK flip-flop sets again with ØKN high and TSMN is made inactive (high).

c) TIMING FOR READ CYCLES WITH ERROR

The basic cycle is exactly as described previously with the following exceptions (refer to Figure 6.10 - Read Word Error).

Data is read out of memory and presented to the ECC where it is latched by CLEC. This uncorrected data is also driven, by ENDATN, to the output buffers H and J and then, by TRDØ(L/R)N onto the BIO lines. But now, some time after T7 goes high, the ECC discovers an error and activates SFN (Single Fail Not - low). Via an AND gate, ENERR now goes high (from SF, RCY and FSM all being high) and as T5 pulse goes low at time T9 sets the ERROR flip-flop. As ERROR goes high so T7ERN (T7 Error Not) goes low (due to ERROR, PWUP and T7 all being high), until T7 drops again at T11. T7ERN causes the parallel input mode of the shift register to last for one more clock thus delaying the earliest possible new cycle time also by one clock. This gives the ECC time to correct the data.

Now it can be seen that ENDATN drives the uncorrected data onto the Bus but now when BUSEC drives there is a very short period when the ECC may be driving corrected (ie., different) data to that driven by ENDATN. By T9 the corrected data should be steady and TRDØ(L/R)N now drives the correct data onto the BIO lines. The biggest effect of the error is to delay TSMN three clocks (goes low at T11 instead of T8). This is because SFN, being low, blocks the AND (of the AND-OR-NOT device) previously used and so the 3-input AND now has to be used. The inputs here are ERROR, T7 and T6N so ENØK is not made low until the end of T6 (T10) thus delaying ØK and TSMN until T11. T12 is therefore the earliest time at which a new cycle may possibly begin.

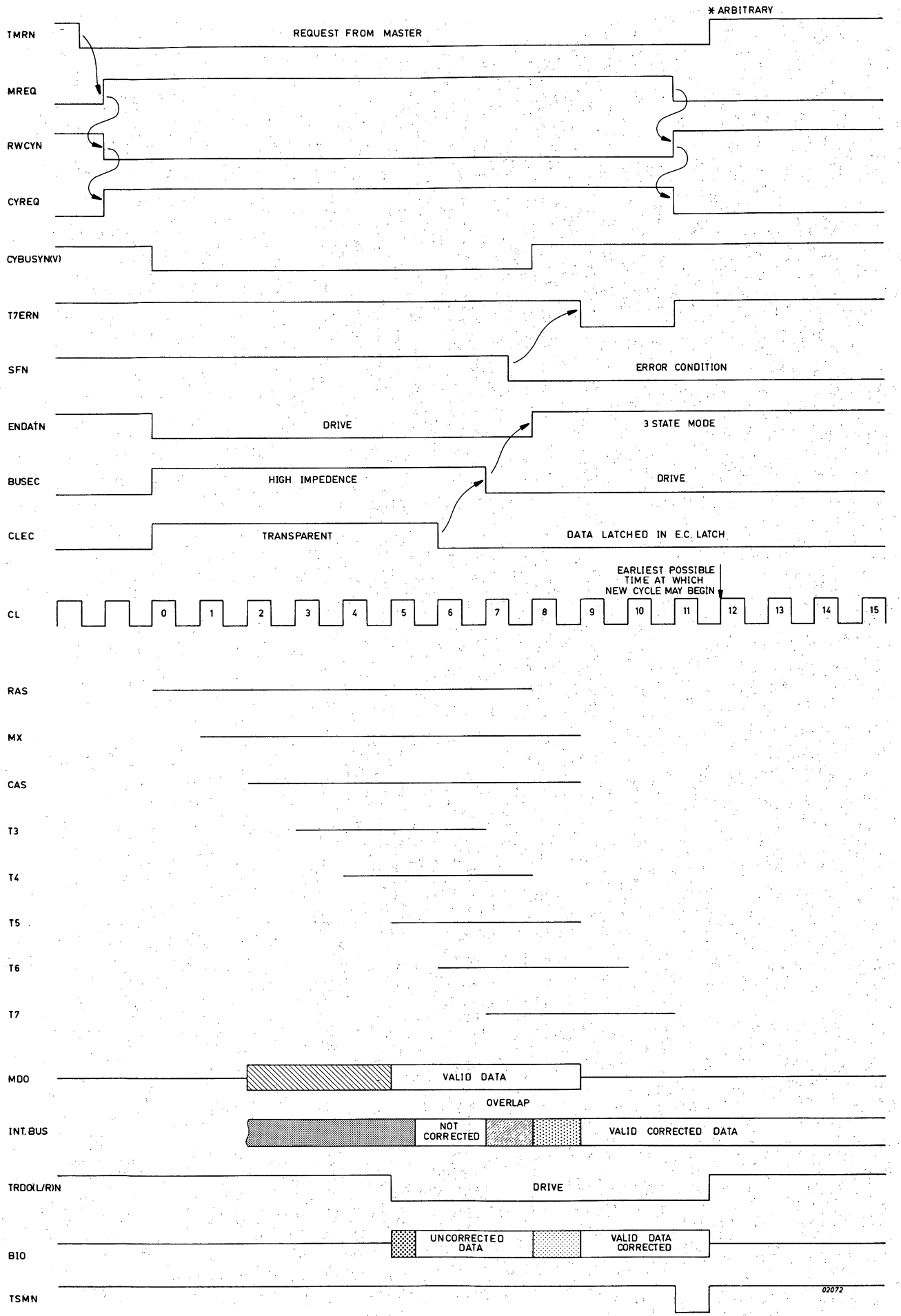


Figure 6.10 READ WORD - ERROR

d) TIMING FOR WRITE CHARACTER

As mentioned previously, a Write Character operation is more complicated than any other because it involves "saving" one character from the addressed location and rewriting it together with the "new" character. This requires two complete, successive memory cycles initiated by the signal RDCY (Read Double Cycle). WRITEV (high during write cycles), RFCUNV (high when not a refresh cycle) and CHAV (high when character mode) are ANDed to form ENDCY (Enable Double Cycle) which is only, therefore, high during a Write Character operation. The cycle begins in the usual way with TMRN enabling ENREQ, MREQ, RWCYN, and CYREQ, and starting up the shift register. As RAS goes high at the beginning of this cycle, CYBUSYN (Cycle Busy Not) goes low in the normal way, followed by CYBUSYNV.

As CYBUSYN goes low it clocks a JK flip-flop with RDCY as its 'K' input and ENDCY as its 'J' input. The flip-flop thus sets, enabling RDCY, so that now both its inputs are high. RDCY also forces MCY low which, in turn, forces WCY low. WCY is gated, at T5, to form WEN for the RAM array, (see diagram 1 - Address Selection) thus, although the signal WRITE is high, which normally forces the RAM's to write, during this first cycle of the double cycle they are forced to read. Through another NAND gate, RDCYN (low) and WRITEV (high) force RWDS (Read Write Double Cycle) high so that the multiplexors D and E select data out (MDØ 0-15) and not data in.

Everything now continues as per a normal read cycle with one other exception. The signal CLLAT (Clock Latch) is normally held low for all other cycles previously described but now, on the read part of the Write Character cycle with RDCY high, CLLAT comes high at T6 (RDCY, T5, and T6). This now forces one of the latches F and G into the Enable and Read Mode, depending upon whether it is a Write Left/Right Character. For a Write Left, ELCH is high thus disabling latch F while latch G is disabled during Write Right by ERCH high. (See Table 6.1 - Data Transfer Signals). The latch that is not disabled then gates the data out character from multiplexor D or E back to the same multiplexor as data in (MDI).

Thus for a Write Left Character; MDI(8-15) are gated back to multiplexor E at the unselected inputs. Note also that at this time the "new" character has appeared on BIO(8-15)N and, for Write Left, has been selected by multiplexor B (due to CHAV being H) which is enabled by ELCHN being low (ERCHN is high, disabling buffer C). Thus the complete new word to be written into memory is available at the inputs of multiplexors D and E towards the end of the first (read) cycle.

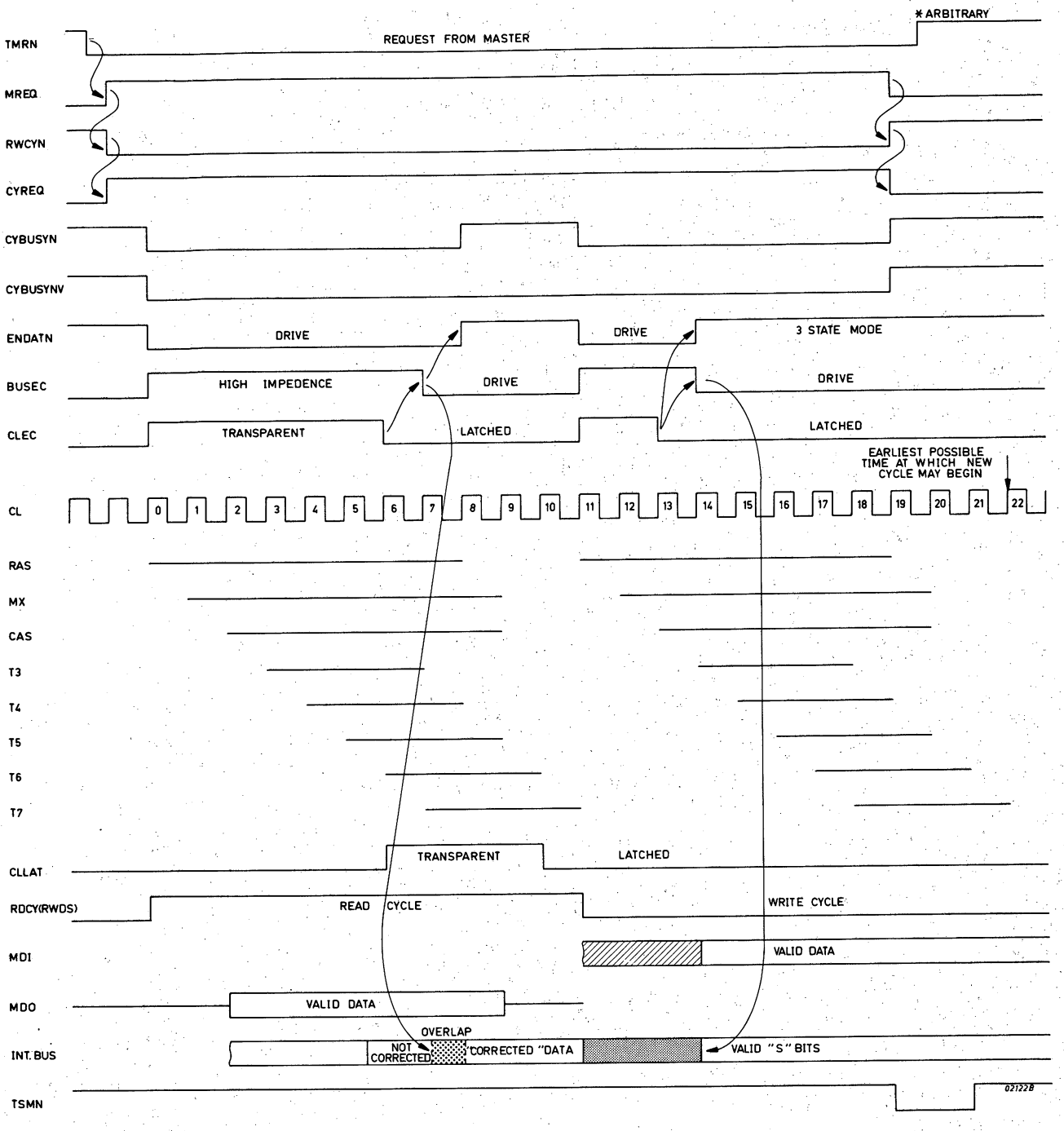


Figure 6.11 WRITE CHARACTER

The remainder of this cycle continues as normal (including the error correction, if required) except that output drivers H and J are disabled (because RCY is low) and no data appears on the BIO lines. when CYBUSYN goes high again at the end of RAS, CYBUSYNV stays low because DCYN (Double Cycle Not) is also low due to PWUP and RDCY both being high. CYBUSYNV disables one of the gates in the refresh logic to prevent a refresh cycle coming between the two parts of the double cycle (see Timing Refresh Cycle).

At the end of the "read cycle", MREQ is still high (because TMRN is still active, not having received a TSMN yet as ENØK is blocked by RCY, MCY and WCY all being low), so the shift register immediately starts up again one clock after it reverts to serial input mode at T10, ERROR having been blocked by RCY being low. As soon as RAS comes high, CYBUSYN goes low and clocks the JK flip-flop which now has both its inputs, ENDCY and RDCY, high. Thus the flip-flop toggles and RDCY goes low, enabling both MCY and WCY to go high. RWDS now goes low and CLLAT is disabled (low) again. Thus a normal write word cycle takes place with RWDS now selecting the MDI inputs of the multiplexors D and E, which contain the data for the new word as previously described. This time, ENØK is enabled by WCY so TSMN gets sent at T19 of the complete cycle and CYBUSYNV goes high with CYBUSYN at the end of RAS to allow a refresh cycle. (The full description of the Write Word Cycle is in paragraph b of the Timing Read/Write Cycle.

6.7 TIMING REFRESH CYCLE

There are two types of Refresh Cycle, known as Automatic Refresh (AR) and Hidden Refresh (HR) and their relationship can be seen in Figure 6.12 - Refresh Relationship. The 16K RAM's require complete refreshing (for all 16,384 cells) within 2ms. A refresh cycle differs from a normal read/write cycle in that the CASN(0-3) signals are all held high (incative) throughout the cycle. Thus the RAM's require only one 7-bit address, strobed by RAS, and refresh all 128 columns in the addressed row (the internal RAM cell array being 128 rows x 128 columns - see figure 5.2 - RAM Block Diagram). the 128 columns are read out (each column having its own sense amp), and rewritten, this action restoring the full charge which would otherwise leak completely away.

In a refresh action, it is required to refresh each of the 128 rows, in every RAM on the card, within 2ns. With a clock period of 62.5ns, 240 clock pulses elapse in exactly 15µs; thus 128 x 15µs is 1.92ms. So we require a counter which counts up to 240 and, if a refresh is performed at every count 240 then the memory will be refreshed satisfactorily.

However, if a refresh is performed at every count 240 there is a strong possibility that a refresh request may clash with a read/write request. As far as the refresh cycle goes, it is not important to wait even 1.5µs for a Write Character cycle to take place - it will be possible to refresh within the 2ms limit. But the whole PGP Bus will be held up if a master has to wait 700ns or so far a refresh to take place, hence the need for the two types of refresh.

The definitions are as follows:

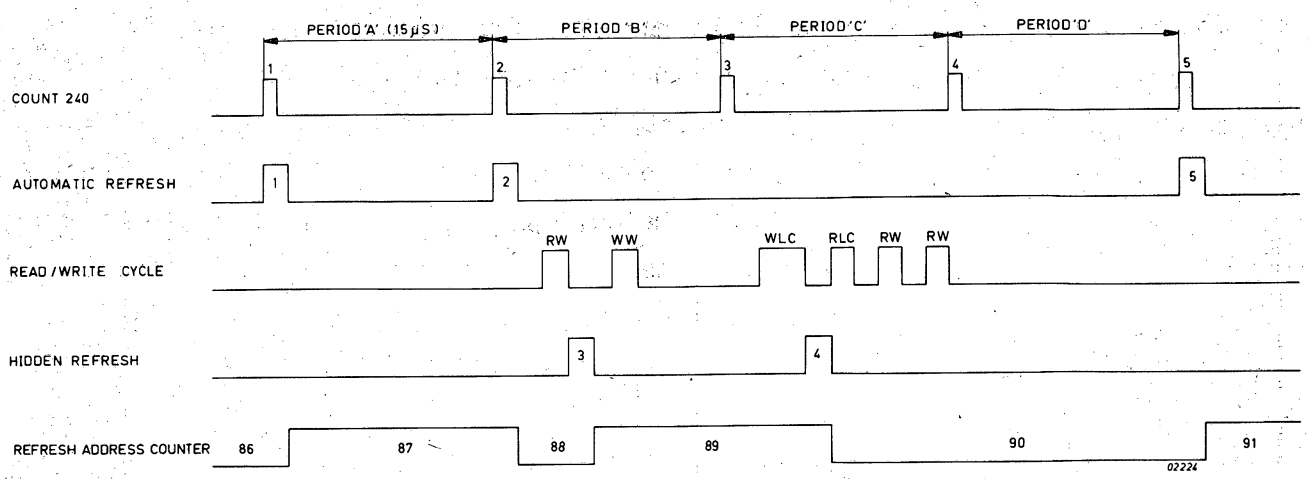
1) Automatic Refresh (AR):
   If there is no read/write request during a 15µs period between two 'count 240's' then a refresh is performed at the end of the 15µs period as in 'A' and 'D' in figure 6.12. This is called an Automatic Refresh (AR).

2) Hidden Refresh (HR):
   If there is a read/write request during a 15µs period between two 'count 240's' then a refresh is performed immediately after the first (and only the first) read/write cycle and the AR at the end of the 15µs period is disabled as in 'B' and 'C' in figure 6.12. This is called a Hidden Refresh (HR) because the refresh can usually be performed before the master can respond to the TSMN and reactivate the TMRN for another read/write cycle. When the memory is busy, therefore, the chance of a master having to wait for the memory to perform a refresh is negligible.

The refresh addresses are completely independent of the read/write addresses and are provided by a Refresh Address Counter which increments the address by '1' at the end of every refresh.

Note that, in figure 6.12, although the refreshes occur at irregular intervals (1-2 = 15µs, 2-3 = 3µs, 3-4 = 15µs, 4-5 = 27µs), there are exactly the same number of refreshes as count 240 pulses because when an HR is performed, the subsequent AR is not, so only one refresh occurs in every 15µs period.

The refresh period is timed by the Refresh Counter which consists of two 4-bit counters linked so that every time counter 1 reaches 16 (the transaction from '1111' to '0000') counter 2 is clocked. Counter 1 is clocked by CLN every 62.5ns so counter 2 is clocked every 1µs.



6.12 REFRESH RELATIONSHIP

When counter 2 reaches '1111' the signal RPCAR1 (Refresh Period Carry 1) goes low via a NAND and, two clocks later as RPCNT1 goes high (count 2 of counter 1) a D-type flip-flop is clocked to force STRFN (Start Refresh Not) high and STRF low. STRFN going high clears counter 2 to '0000' (thus counter 2 counts from '0001' to '1111' which is 15) and STRF going low clocks a JK flipflop with RFRQH as its 'J' input. As we shall see later, if there has been a read/write request during the previous 15μs period, then RFRQH (Refresh Request Hidden) will be low thus preventing the A.R. from continuing any further. If, however, there was no R/W cycle during the previous 15μs period then RFRQH is high and the flipflop forces ERFRQN (Enable Refresh Request Not) low. At this moment we can assume SARFRQN (Set Advance Refresh Request Not) to be high (inactive) as will be shown later. Therefore, via a NAND gate, JRFRQ (J Refresh Request) goes high. At the next CLN, JRFRQ forces ARFRQ (Advance Refresh Request) high and, one CLN later still, RFRQ (Refresh Request) goes high. (Refer to figure 6.13- REFRESH).

At this point, the refresh may be held up if a R/W cycle is taking place, or is about to take place by an AND gate with inputs RWCYN (Read/Write Cycle Not - inactive high), CYBUSYNV (Cycle Busy Not-inactive high) and RFRQ. If all is well, RFE (Refresh Enable) goes high and, in successive clocks, ARFCY (Advance Refresh Cycle) and RFCY (Refresh Cycle) both go high. ARFCY going high disables the R/W Address Multiplexor, ARFCYN going low enables the Refresh Address Counter address to the memory array as A(0-6), RFCYN going low enables both the RAS (0/1)N strobes on a 32K card while RFCYNV (basically the same signal) forces CASN(0-3) all high. RFCYN going low also forces CYREQ high and starts up the shift register. The timing is exactly the same as for a normal "short" cycle but the RAM's realise this is a refresh and not a R/W cycle because CASN(0-3) are held high throughout the cycle.

Meanwhile, STRF has gone high again as the flipflop "resets" due to RPCAR1 being high (counter 2 having been reset as described previously) and RPCNT1 going high again at count 6 of counter 1. STRF going high clocks another D-type flipflop to ensure that RFRQH (Refresh Request Hidden) is high. Note that, as this description applies to an AR, then RFRQH would be high anyway, since there would have been no R/W cycle to reset it (described below). Had the count 240 followed a period during which there had been a R/W cycle, RFRQH would be reset at this time to enable a H.R. during the next 15µs period. The A.R. would then be disabled as previously described.
The A.R. cycle ends as follows. ARFRQ is reset as the ARFRCY flipflop sets (due to ARFCYN going low). ERFRQN and RFRQ are reset at T5 by RRFRQN (Reset Refresh Request Not), RFE is reset (made low) by RFRQ, and ARFCY follows one clock later. RFCY is reset by CAS going low, forcing RRFCYN (Reset Refresh Cycle Not) low and resetting the flipflop. If, during a refresh cycle a R/W request became active due to TMRN going low, it is held up by RFRQN being low. But RFRQN goes high (thus enabling RWCYN to go low) before RFCYN goes high, thus CYREQ remains high and the R/W cycle takes place one clock. After the refresh, when the shift register reverts to serial input mode at T10.

As this R/W cycle is now the first of the new 15µs period it generates a H.R. as follows. At time T3 of the R/W cycle, SARFRQN (Set Advanced Refresh Request Not) goes low due to all four NAND inputs being high (RFCYNV because it is not a refresh cycle, RFRQH because it either was high already or was set at the last count 240, T3 from the shift register and DCYN which just prevents the refresh from occuring between the two cycles of a Write Character Operation). SARFRQN going low enables JRFRQ via a NAND (ERFRQN is high at this time) and so begins the sequence of events already described leading up to a refresh cycle immediately following the R/W cycle. However, when ARFRQ becomes high, RRFRQHN (Reset Refresh Request Hidden Not) goes low (ERFRQN is still high) thus resetting RFRQH and disabling the NAND so that any further R/W cycles will not enable SARFRQN and so start refresh cycles. RFRQH now remains low until the next count 240 at which no A.R. is generated (because RFRQH is low) but then RFRQH is reset to enable the H.R. for the first R/W cycle of the following 15µs period.

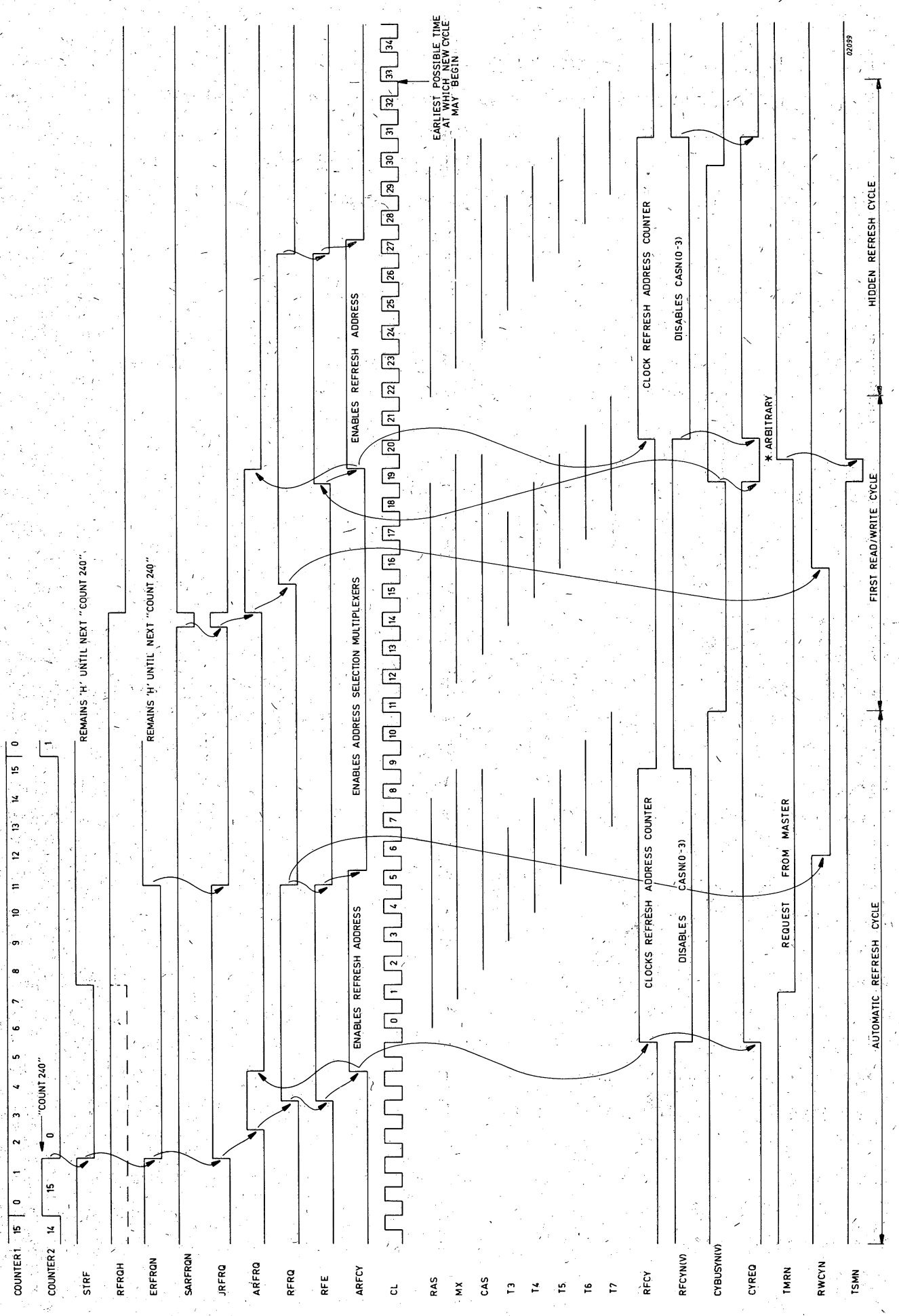


Figure 6.13 REFRESH

6.8 POWER AND BATTERY BACKUP

As described elsewhere in this manual, the memory is supplied with +5V and +12V during 'normal run mode'. From the +12V there is circuitry on the WMA-1 PCB to generate the -5V required for the RAM devices (see diagram 1 - -5V FORMATION). 'Normal run mode' is defined at the memory interface by RSLN being high (see diagram 3 - TIMING READ/WRITE A).

In case of a power failure the P4500 system may be put into "standby mode" when the required voltages provided by the Backup Battery Module. On the logic diagrams, all devices marked with a "B" are provided with +5VM from the B.B.M. - the RAM's are also supplied with +12VM which produces -5V.

Thus it can be seen that all the refresh and addressing logic is enabled but none of the data control devices or their timing and control signals. If system power is removed then, the battery backup ensures that the information in the memory is not lost.

6.9 P851 MODE

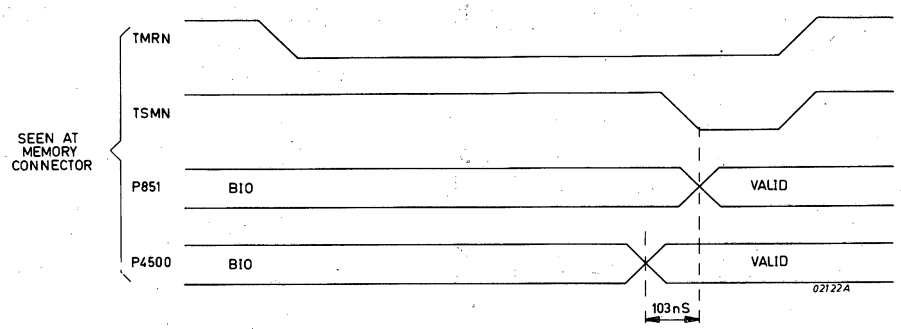
If the WMA-1 PCB is used in a P851 system, or if any Master or Slave in a P4500 system is of the "old" (P851) type, then the strap indicating the mode must be set pin 1-2 (indicating P851 mode - see Strap Setting).

This has the effect of enabling the signal ENØK at T8 and ØK one clock later (see diagram 3 which means that effectively TSMN is not sent until T9 (one clock later than FSM mode with no error) but is always sent at T9. Thus only the "short-cycle" is used as signal FSM being low disables ENERR and, therefore, T7ERN.

Also, P851M being high enables S851M to be low as CLEC goes low during a read cycle. This means that ENDATN stops driving (goes high) at the same time as BUSEC goes low to drive the E.C.C. output. The output of the E.C.C. is initially uncorrected but BUSEC is driving corrected data onto the BUS before TSMN goes active at T9. (see figure 6.14 - P851 MODE READ WORD).

Note that Write Word and Read cycles are similar in P851 mode but different from FS mode and the Write Character cycle is composed of a 'Read Word' and a 'Write Word' Double Cycle in the same way as FS mode but with the slightly different timing.

This basic timing differences is neccessary because of the different ways in which the BIO lines are handled by P4500 and P851 as in the following relationship:-



In P851, the data on the BIO lines must be valid at least 0ns before TSMN is activated (seen at the memory connector). The Master must then create its own delay (typically 100-200ns). In P4500, data must be valid at least 25ns before TSMN (seen at the master) in order to clock the BIO lines into the Masters buffer (this is about 103ns seen at the memory consector).

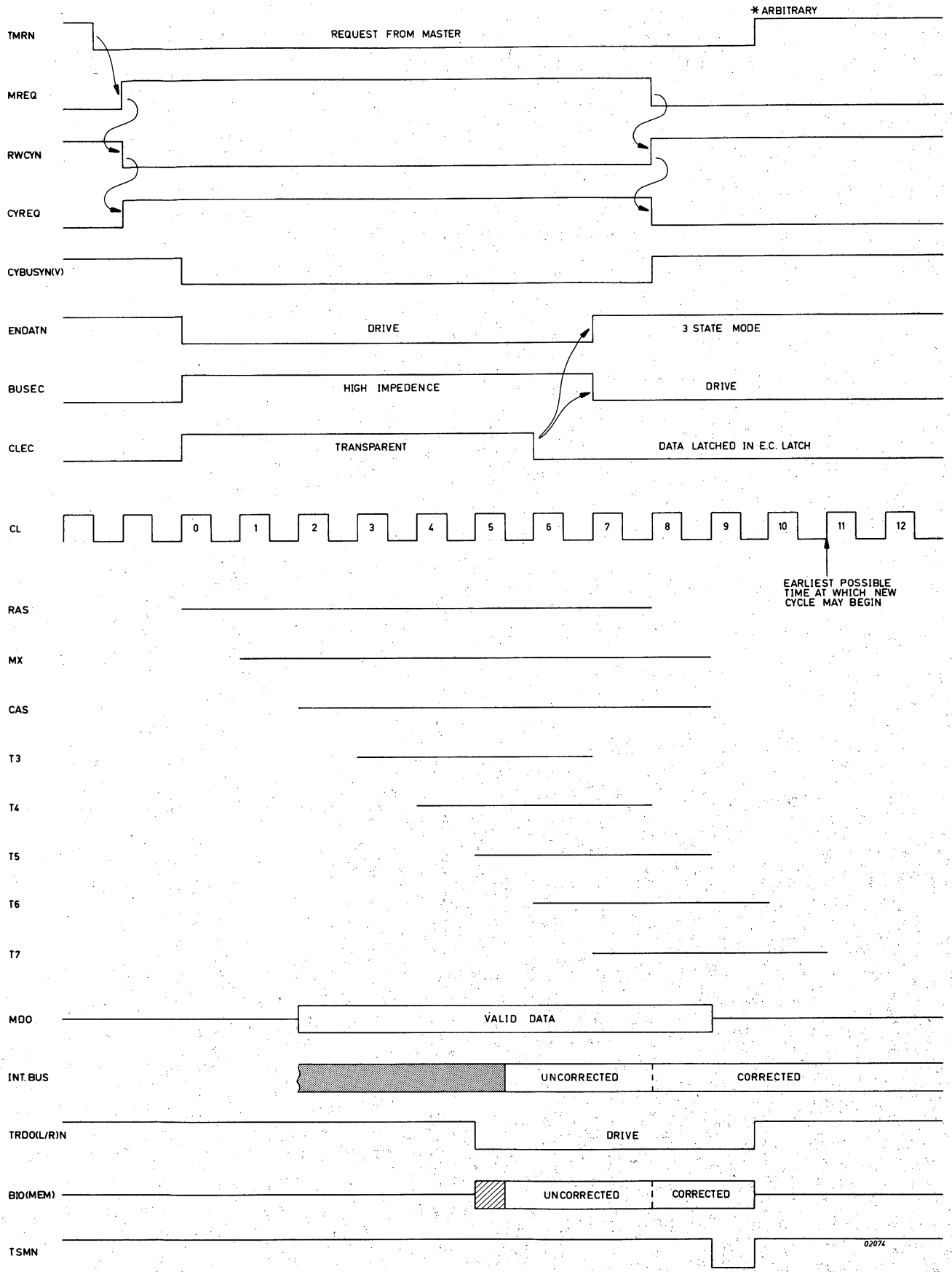


Figure 6.14 P851 MODE READ WORD

CHAPTER 7 DIAGRAMS

Figure 7.1 MEMORY ARRAY PAGE 7-3
- ADDRESS SELECTION
- -5V FORMATION

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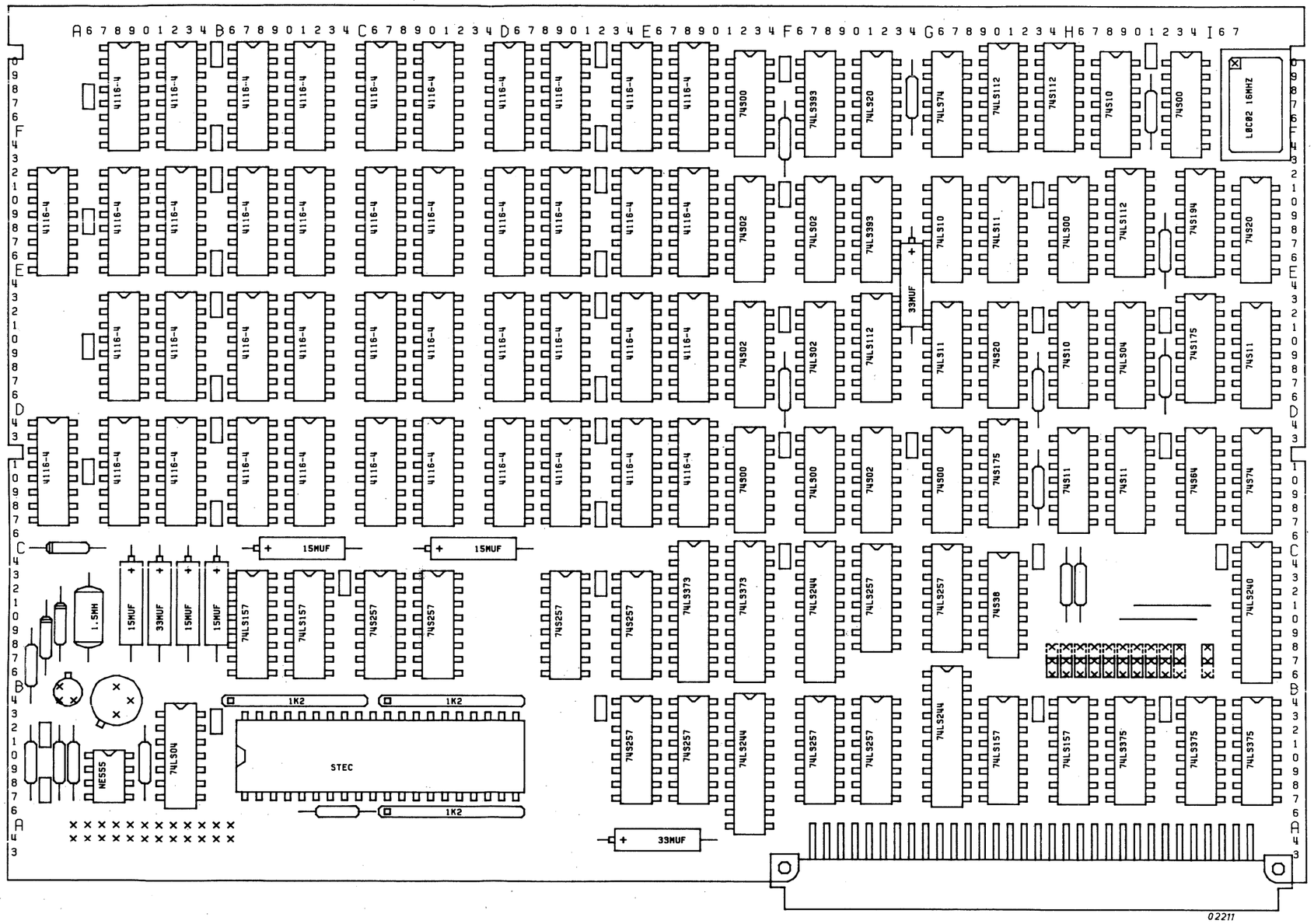
- TESTPOINTS ADAR
- DATA IN
- DATA OUT

Figure 7.3 TIMING READ/WRITE CYCLE A 7-7
- TIMING READ/WRITE CYCLE B
- TIMING REFRESH CYCLE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74LS00
74LS112
74S194
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74LS02
74LS112
74LS11
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1.5MH
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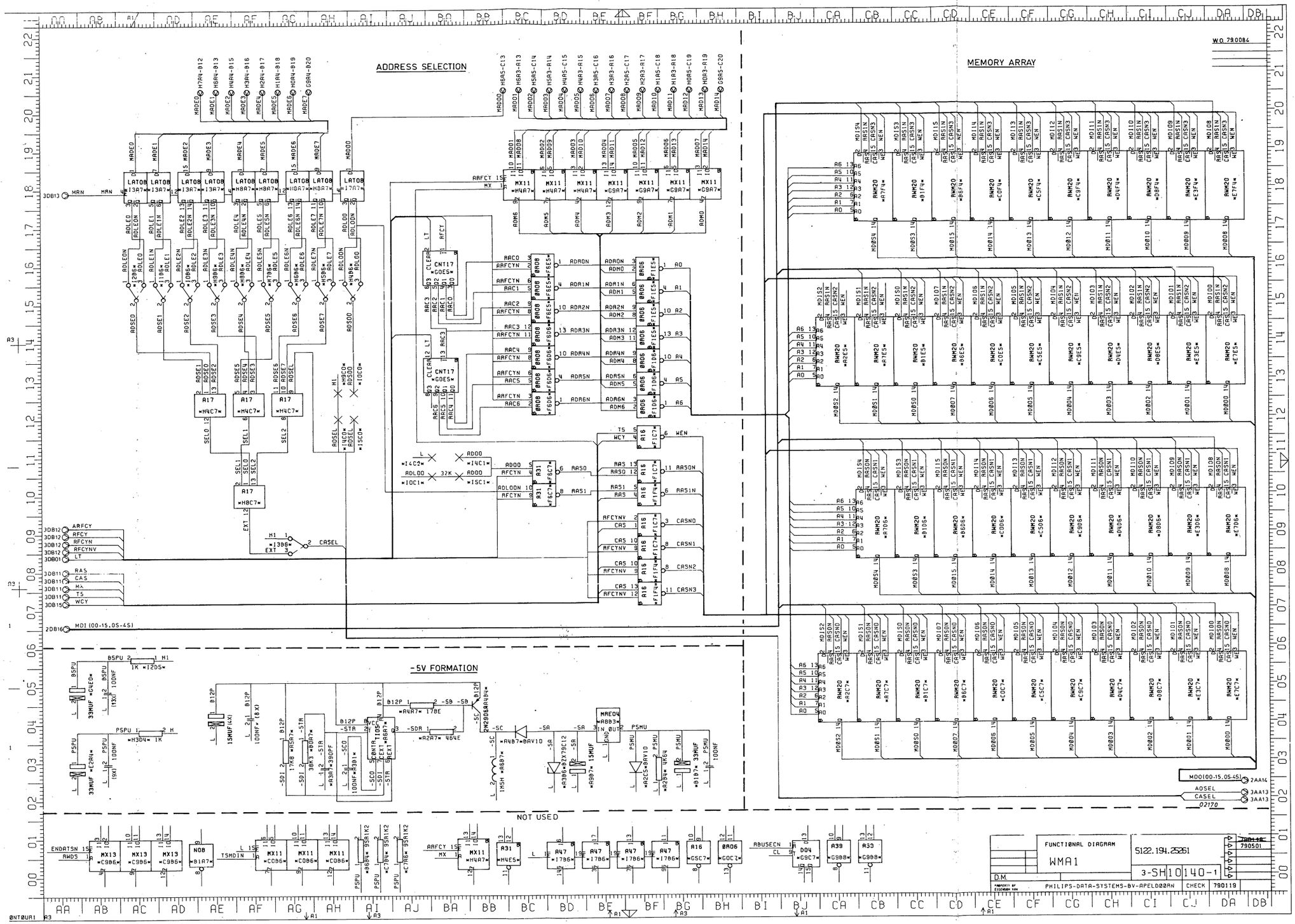
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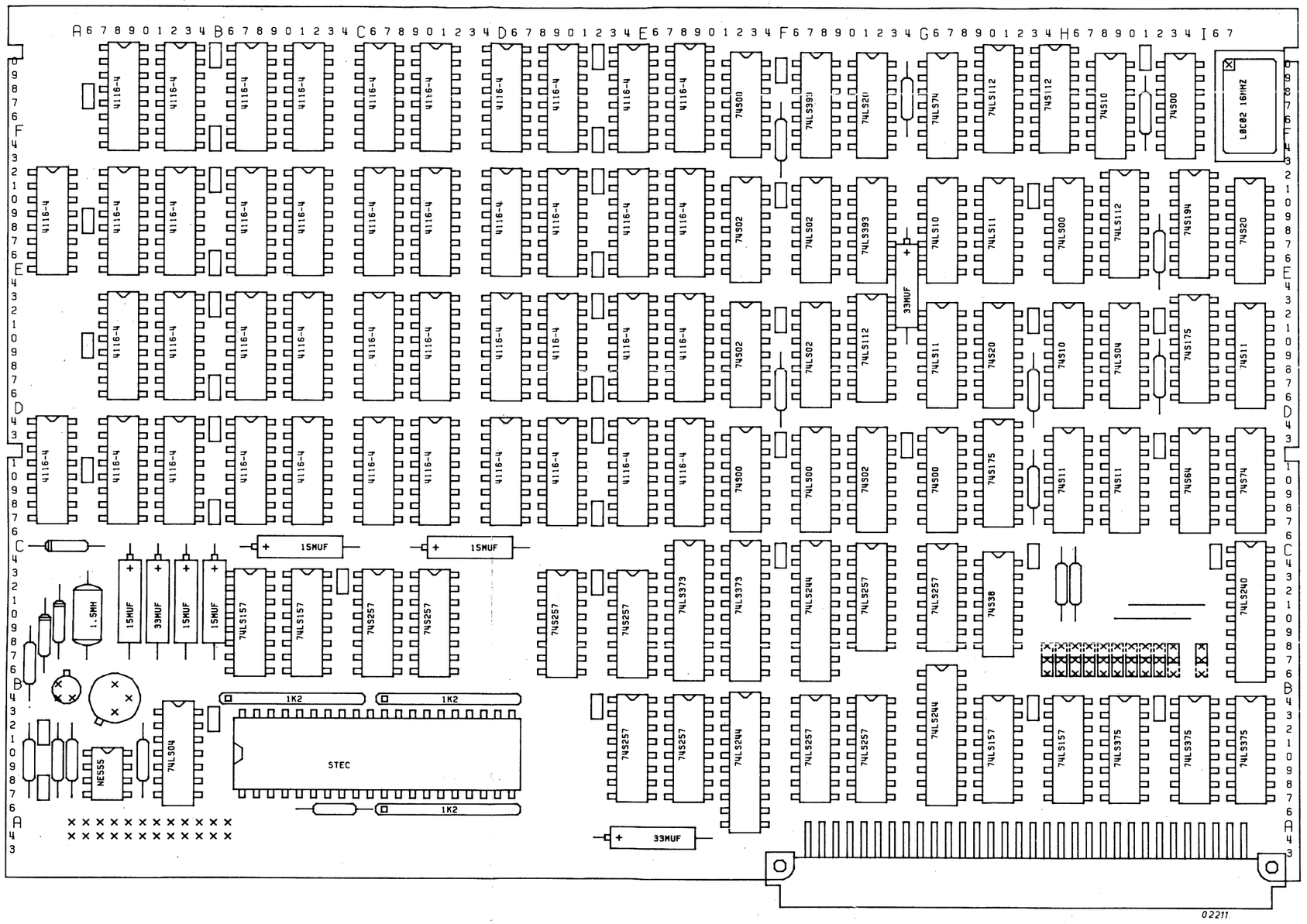
CHECK 790119
790501

Figure 7.1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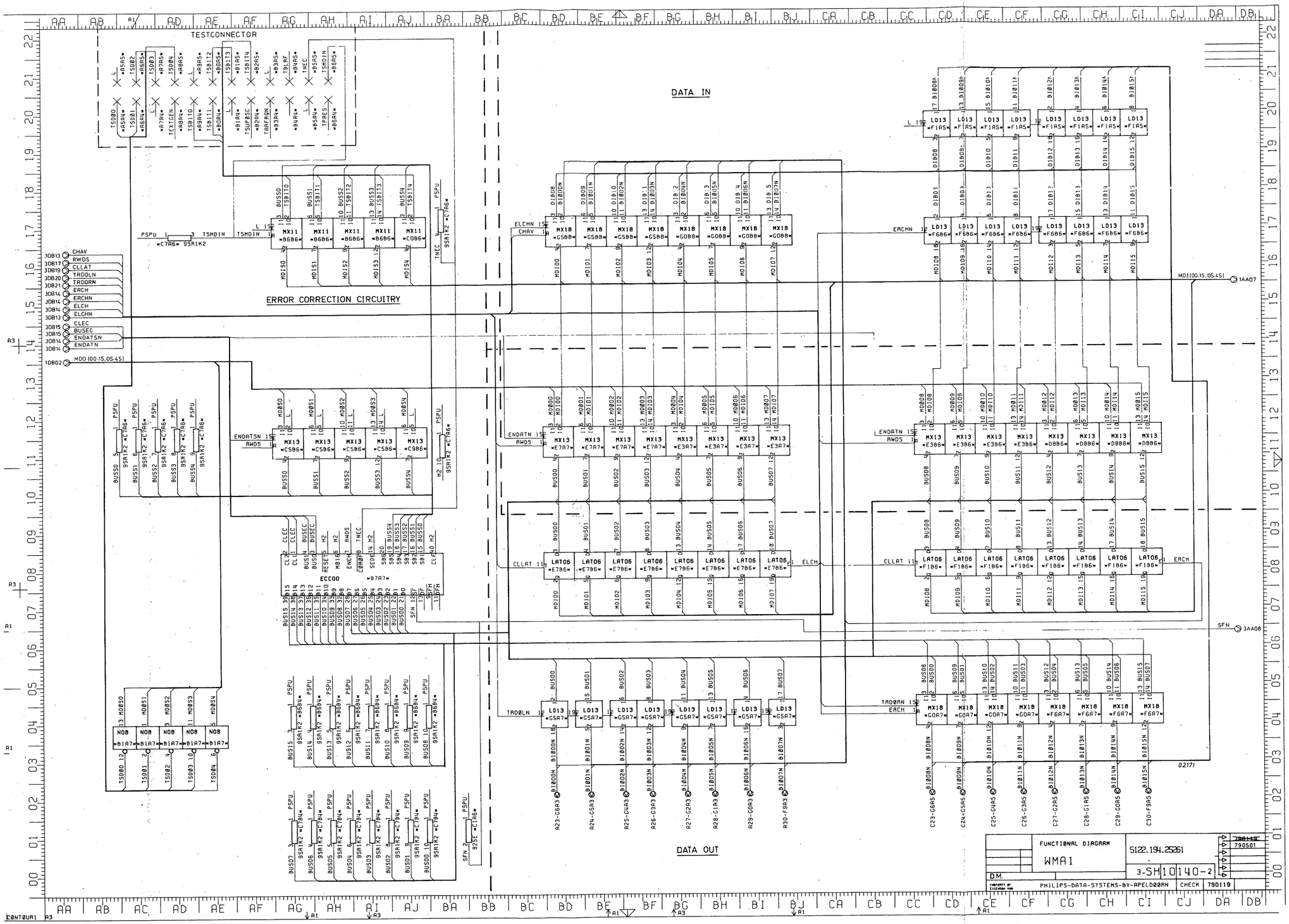
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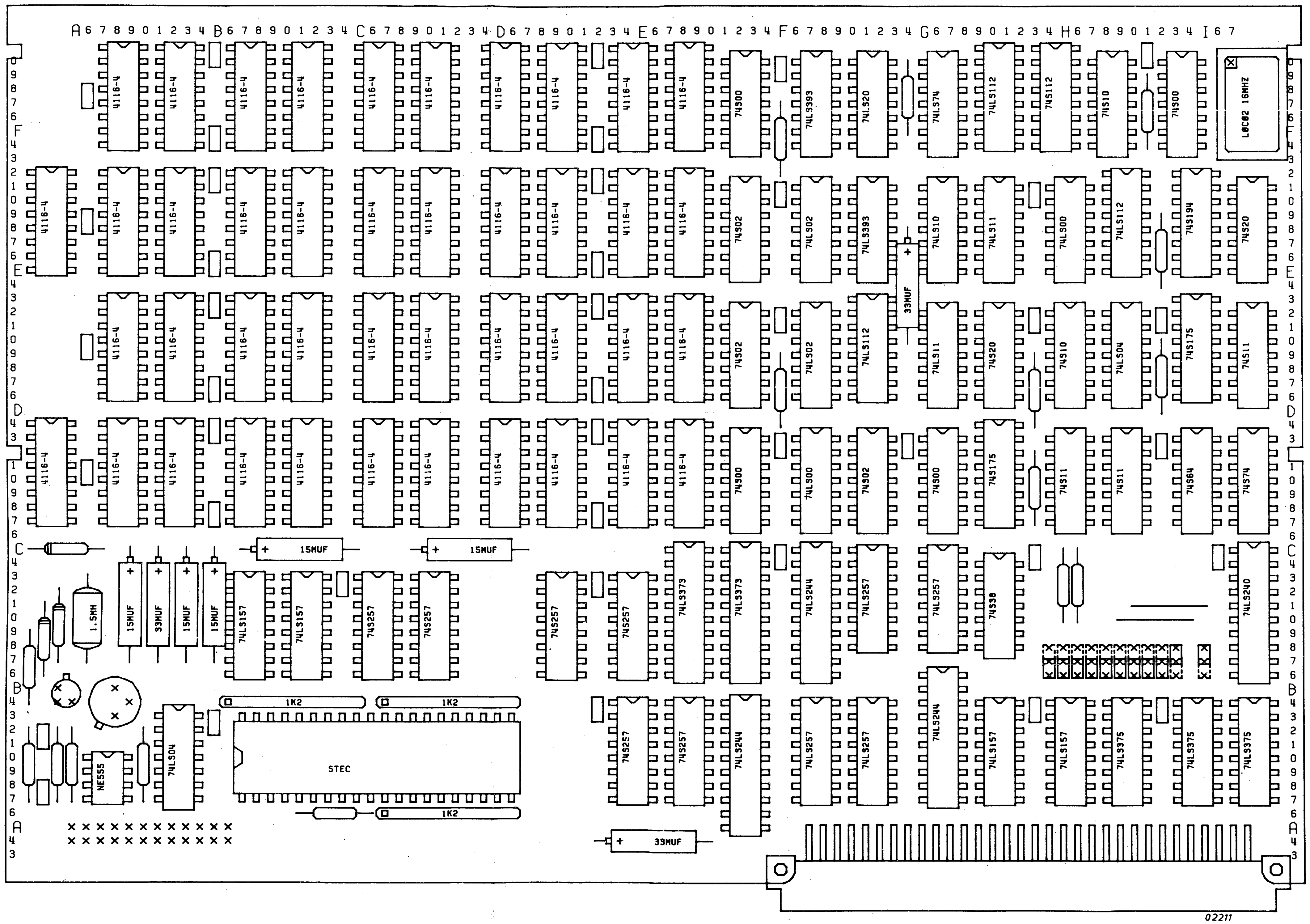
Figure 7.2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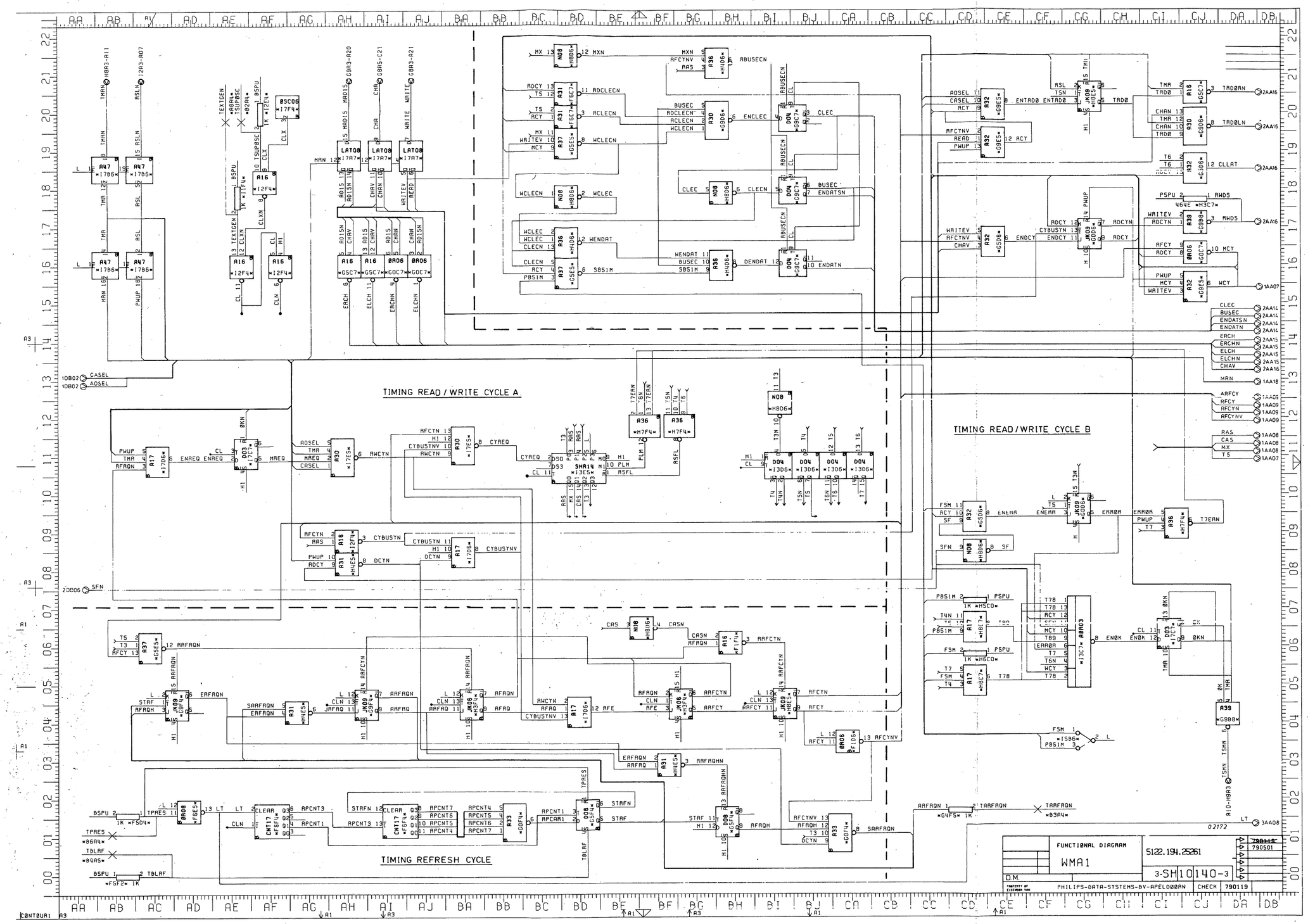
TIMING READ / WRITE CYCLE A
TIMING READ/WRITE CYCLE B
TIMING REFRESH CYCLE
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790501
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Figure 7.3